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(71) Applicant *(for all designated States except US)*: **SEMITOOL, INC.** [US/US]; 655 West Reserve Drive, Kalispell, MT 59901 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **RITZDORF, Thomas, L.** [US/US]; 3130 Parkwood Lane, Bigfork, MT 59911 (US). **FULTON, Dakin, J.** [US/US]; 2365 Poplar Place, Whitefish, MO 59937 (US). **CHEN, Linlin** [CA/US]; 3213 Placid Springs Lane, Plano, TX 75025 (US).

(74) Agent: **KELBON, Marcia, S.**; Christensen O'Conner Johnson & Kindness PLLC, Suite 2800, 1420 Fifth Avenue, Seattle, WA 98101 (US).

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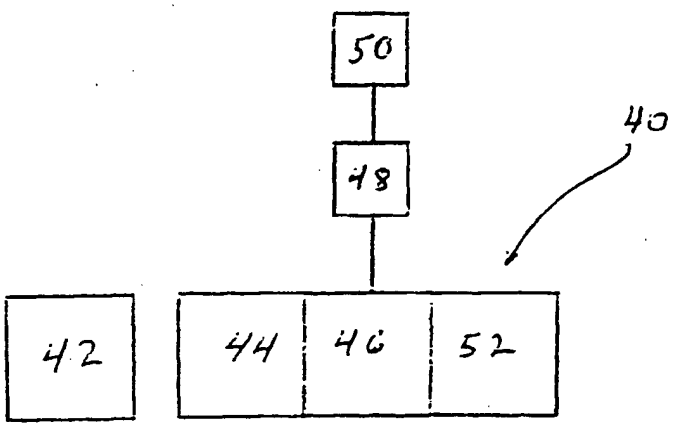

(57) Abstract: A process for depositing a metal structure, such as copper interconnects, on a surface of a workplace, such as a semiconductor wafer, the workpiece surface defining a plurality of recessed microstructures. The surface of the workpiece is exposed to an electroplating bath including copper ions to be deposited on the surface and an organic additive that influences the metal ions to be preferentially deposited within the recessed microstructures relative to the remainder of the surface. Electroplating power is then provided between the exposed surface of the workpiece and the anode for a first time period such that the copper ions are deposited on the surface and nominally fill the recessed microstructures. The electroplating power is then reversed between the anode and exposed surface of the workpiece during at least a portion of a second time period to limit the deposition of further copper over the nominally filled recessed microstructures, relative to the remainder of the surface, to ameliorate the development of a "momentum plating" overburden bump of metal over the recessed microstructures. In a preferred embodiment, the reverse electroplating power is supplied in a series of reverse power pulses interspersed with forward power pulses. In addition to the pulsed reverse power application reverse power may also be applied during a sustained time period. An apparatus is also provided for carrying out the process utilizing reverse power application to ameliorate momentum plating bump formation.

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PATTERN DEPENDENT SURFACE PROFILE EVOLUTION OF ELECTROCHEMICALLY DEPOSITED METAL

Cross-Reference to Related Application

The present application claims the benefit of United States Provisional Application 60/155,959 filed September 24, 1999.

Field of the Invention

The present invention relates to electrochemical deposition of metals on workpieces that define recessed microstructures.

Background of the Invention

Processes for manufacture of microdevices, such as integrated semiconductor chips and micromechanical devices, often entail application of metal interconnect structures to a substrate. In recent years, techniques for producing semiconductor devices in particular have utilized deposition of copper interconnect structures onto a semiconductor substrate. In one technique, referred to as damascene electroplating, an insulator substrate is patterned to define recessed microstructures, such as trenches (lines) and vias (holes). FIGURE 1a provides a schematic illustration of the surface of a workpiece 10 including an insulator layer 12 into which recessed structures 14 have been formed. A barrier layer 16, such as titanium nitride or tantalum nitride, is typically applied to the insulator to prevent migration of a subsequently applied metal (in the case of copper) into the insulator. Because of limitations in electrochemical deposition of metals onto the barrier layer in a uniform conformal layer, it is typically necessary to first apply a seed layer 18 of metal onto the barrier layer (although a seed layer may be eliminated in certain applications). The seed layer is often deposited by a

chemical vapor deposition technique, or alternately by a physical vapor deposition technique. Additional metal 20 is then applied to the seed layer using electrochemical deposition to fill the recessed microstructures, as well as the surrounding surface (the "field") with a conformal metal coating. Thereafter, the deposited metal is removed from the field, such as through use of a chemical-mechanical polishing technique (CMP) or other planarization step, leaving the metal-filled trenches, vias or other field recessed microstructures (FIGURE 1b).

A difficulty that has been experienced in electrochemical deposition of metals onto substrates is the tendency of the metal to preferentially deposit onto the surrounding field surface rather than on the bottom and sides of the microrecessed structure, due to greater mass transfer outside of the recessed structure. This can result in undesirable voids or seams being formed in the metal that fills the recessed structure, undesirably increasing the resistivity of the filled structure. Techniques have thus been developed for manipulating the deposition of metal so that the metal is preferentially deposited in the recessed microstructures during electroplating, through the incorporation of organic additives in the electroplating bath.

With respect to electrochemical deposition (ECD) of copper for metal interconnects and devices, organic additives utilized to completely fill submicron recessed features typically have the role of either suppressing or enhancing metal deposition, based on the local additive concentration. The widespread acceptance of ECD processes as the standard deposition method for filling etched features to produce inlaid interconnects is due in large part to the fact that ECD is the only method to date capable of depositing preferentially inside the features, a characteristic that has been called "superfilling." Andricacos, P.C. et al., *ULSI Fabrication I and Interconnect and Contact Metallization: Materials, Processes, and Reliability*, ECS Proc. 98-6.

Optimization of the use of organic additives involves understanding the effects of each constituent on the properties of the deposited film, including the fill capability for deep submicron features, the electromigration resistance of the interconnect, and the deposited film topography. When optimizing the additives for feature fill capability, it becomes apparent that topography is also strongly affected. A typical electrodeposited copper film is presented in FIGURE 2. When using organic additives to preferentially fill recessed microstructures, a phenomena is exhibited in which deposited metal overfills the recessed

microstructure, forming an overburden of metal above the recessed features. As seen in FIGURE 2, overburden "bumps" on top of the feature can be observed. Bump heights are strongly dependent on the feature size and feature density, with large bumps on top of the small, dense features. Since the conventional next step after electroplating is CMP to planarize the wafer surface, these pattern-dependent bumps can lead to uniformity problems for the CMP process. CMP may differentially polish areas of the substrate due to the raised bumps, as further complicated by different grain structures for the bumps and surrounding areas.

The effect seen in FIGURE 2, which has been referred to as a "momentum plating" effect, is very interesting, in that initial concave features have been turned into convex topography. While this behavior may seem counterintuitive, it is theorized (without limitation) to be a relatively straightforward result of the additives that have been used to produce the super-conformal deposition profile, which is desired in the filling of deep sub-micron inlaid features.

The ability to fill deep sub-micron, high aspect ratio features used in inlaid copper interconnect technology is largely determined by the presence of organic additives to modify the electrolytic deposition process. Although there are a large number of names that have been used to describe these organic additives, they can be generally classified in two groups. These categories are suppressors and accelerators, and are named after the effect they have on the deposition rate at a given deposition potential. Conventional wisdom holds that the suppressors typically adsorb preferentially to the surface of the wafer in the field area, compared to the insides of the recessed features. This is theorized to be due to an elevated diffusion coefficient for these large molecules inside the. microscopic features: K. Takahashi et al., *Advanced Metallization Conference (AMC 1998)*, edited by G.S. Sandu, et al., Mater. Res. Soc. Proc. ULSI XIV, Pittsburgh, PA 1998, p. 57-63; M.E. Gross, et al., *Advanced metallization Conference (AMC 1998)*, edited by G.S. Sandu et al., Mater. Res. Soc. Proc. ULSI XIV, Pittsburgh, PA 1998, p. 51-56. The accelerators, which are usually small molecules, are then free to adsorb on the interior of the feature, and accelerate the deposition rate locally.

This effect, which results from the organic additives used in the copper plating bath, can be utilized to develop what is referred to as a "bottom-up" deposition profile (FIGURE 3). This means that the deposition rate within the etched feature, and especially at the bottom, is much greater than the deposition

rate on the surrounding top surface, or field area. It is exactly this ability of organic additive interaction that provides greater than 100% step coverage, or super-conformal deposition. This super-conformal deposition allows high aspect ratio, or even re-entrant, trenches to be filled without a seam. FIGURES 3 and 4 demonstrate such a "bottom-up" fill sequence for vias and trenches, respectively, by use of conventional ECD copper plating techniques in a copper sulfate bath including accelerator and suppressor additives.

As can be seen, the trenches were preferentially filled during the initial deposition (FIGURE 4a) and the preferential deposition in the vicinity of the inlaid feature does not stop once the copper surface has become planarized (FIGURES 4b and 4c). It is almost as if the deposition process exhibits a "momentum" that carries this increased deposition rate over the nominal surface to produce a convex feature where there was initially a concave one. This effect is believed to be unique to electrodeposition in the presence of organic additives. Some clue as to the mechanism behind this effect can be derived from the fact that the bump height generated over a set of features is pattern dependent and exhibits a behavior similar to the pattern-dependent "loading" effect seen in plasma RIE processes.

The pattern dependence of the bump height formed during conventional plating in a copper sulfate bath using accelerator and suppressor additives can be seen in FIGURE 5, and represents the difference in copper thickness between the area immediately above a set of etched trenches and the field copper thickness, as measured using a stylus profilometer. As seen in FIGURE 5, the bump height is strongly dependent on the dimensions associated with the underlying features as well as with the recipe used to plate the copper film. With a first set of plating process parameters (S_2) the highest bump height of 2 μ was obtained on the smallest trench (0.5μ) with a smallest pitch size of 1μ. The bump height decreased as the trench size increased. For the same trench of 0.5μ, the bump height was reduced roughly from 2μ to 1μ when the pitch was increased from 1μ to 2μ. This indicates that there is an interaction between the bump height and the feature and pitch widths. For comparison, the bump heights as a function of trench and pitch widths, which was obtained from a second set of plating process parameters (S_1) with the same organic additives, are also included in FIGURE 5.

While not wishing to be limited to theory, a mechanism has been proposed which demonstrates the physical effects associated with the topography of the

features that are produced by the momentum effect. If the suppressor adsorbs to the field area, above the etched features, and the accelerator is able to diffuse into the features and promote deposition there, it is not difficult to understand how the raised features may be formed. As illustrated in FIGURE 6a, the accelerator ("A") is more concentrated inside the feature due to the inability of the suppressor ("S") to migrate to this area, and its occupation of the active sites in the field region. The suppressor does continue to diffuse into the feature at some rate, however, where it is incorporated into the film as copper is deposited: K. Takahashi and M.E. Gross, in *Advanced Metallization Conference (AMC 1998)*, edited by G.S. Sandu et al. (Mater. Res. Soc. Proc. ULSI XIV, Pittsburgh, PA 1998), p. 57-63; M.E. Gross et al., *Advanced Metallization Conference (AMC 1998)*, edited by G.S. Sandu et al. (Mater. Res. Soc. Proc. ULSI XIV, Pittsburgh, PA 1998), p. 51-56. This causes a localized depletion in the concentration of the suppressor near the feature top, and a relative abundance of suppressor over the majority of the field region of the wafer. Because this creates a situation as illustrated in FIGURE 6b, where the concentration of suppressor very near the feature opening is depleted at the moment the surface becomes planar, the deposition rate in this area is greater than that in the field region. This dynamic situation caused by the diffusion gradients in the system provides a possible explanation for the momentum plating effects typically observed.

If the mechanism is as discussed in the preceding paragraph, one should expect to see the bumps eliminated by simply pausing the deposition at or near the point of planarizing the features for a time sufficient to allow diffusion to create a uniform surface concentration of additives, then proceeding with the deposition. In fact, when the inventors perform this experiment, there is surprisingly little or no effect on the bump height above the trenches found, as described below with respect to the present invention. The inventors have found that in developing the present invention, that the wafer (workpiece) can be completely removed from the plating solution, rinsed and dried, then returned to the reactor for completion of deposition, with no obvious reduction of the bumps. This indicates that a property of the deposited film itself contributes to the profile evolution. The inventors postulate, without limitation by theory, that it is the incorporation of the additives in the copper film as it is being deposited that causes the effect to be so persistent.

The incorporation of the additives into the film as it deposits is represented in FIGURES 6a and 6b, with the exception that this mechanism does not rely on

the dynamic concentration gradients to produce the effect discussed herein. In this case the additive species may remain at or near the surface and continue to accelerate or suppress the local deposition rate, or an affinity of accelerator in the solution for the accelerator incorporated into the film could produce a similar effect. The inventors theorize that the accelerator, in particular, is carried at the surface of the depositing film, where it continues to aid in the deposition of copper in the areas where it has the greatest concentration (i.e. immediately over the features). Byproducts of the accelerators may also be incorporated into the substrate and cause this effect.

Another possible mechanism for bottom-up deposition and bump formation may be related to the interaction of chloride included in conventional copper sulfate plating baths and suppressor. For such plating solutions, the chloride concentration is in the ppm level, and a concentration gradient can be easily formed inside small features. It is known that the suppressor needs to interact with chloride to provide suppressing effect: J.J. Kelly and A.C. West, *J. Electrochem. Soc.*, **145**(10), p. 3472(1998) and **145**(10), p. 3477(1998). Therefore, the concentration gradient of chloride could lead to enhanced deposition rate in the feature. If the interaction rate between the suppressor and chloride is slower than the generation of fresh copper surface, the copper deposit on top of the feature continues to grow to form the bumps.

Conventional techniques for controlling momentum plating entail modifying the additive package in order to reduce the size of the bumps over interconnects. There are two approaches that are feasible. The first approach is to modify the suppressor and/or accelerator to reduce the effect, and the second is to add an additional leveling component to the additive package. In practice, each of these methods tends to degrade the ability of the chemistry to fill very high aspect ratio features, which is an unacceptable tradeoff in order to produce improved post-polish interconnect thickness uniformity. FIGURE 7 compares the effect of a leveling agent on bump formation and gap fill. In the absence of leveling agent, good gap fill was achieved for both large and small features as shown in FIGURES 7a and 7b. After adding leveling agent, although the bump was reduced (FIGURE 7c and FIGURE 7d), tiny seam voids were observed in small trenches (0.18μ 4.9:1AR) in FIGURE 7c. This implies that a degradation in gap-fill was caused by the presence of the leveling agent in the plating solution. Furthermore, the presence of an additional organic leveling agent significantly

complicates the additive package, making it difficult for on-line analysis and control of individual components.

Summary of the Invention

The present invention provides a process for depositing a metal structure on a surface of a workpiece defining a plurality of recessed microstructures. A surface of the workpiece is exposed to an electroplating bath. The bath includes a source of metal ions to be deposited on the surface, and an organic additive that causes the metal ions to be preferentially deposited within the recessed microstructures relative to the remainder of the surface. Forward electroplating power is supplied between the exposed surface of the workpiece and an anode disposed in electrical contact with the electroplating bath for a first time period, so that the metal ions are deposited on the surface. Then the electroplating power supplied between the anode and the exposed surface of the workpiece is reversed during at least a portion of a second time period, to control the deposition of future metal ions over the recessed microstructures relative to the surrounding surface.

In a preferred embodiment of the invention, the process is used for electrochemical deposition of copper or other metals into recessed features of substrates used in the manufacture of integrated semiconductor devices.

In a further aspect of the invention, the forward electroplating power is provided during the first time period at a first level, so that the metal ions are deposited to nominally fill the recessed microstructures. Then, during the second time period, the electroplating power is reversed and supplied at a second level to limit the deposition of further metal ions over the filled recessed microstructures relative to the remainder of the surface, ameliorating the development of an overburden of metal over the recessed microstructures.

In a still further aspect of the present invention, a process is provided for depositing a metal structure on a surface of a workpiece defining a plurality of recessed microstructures. The process entails exposing the surface of the workpiece to an electroplating bath including a source of metal ions to be deposited on the surface, and then supplying forward electroplating power between the exposed surface of the workpiece and an anode disposed in electrical contact with the electroplating bath for a first period of time, and under a first set of plating process parameters, such that metal ions are preferentially deposited within the recessed microstructures relative to the surrounding surface. Then electroplating power is supplied between the anode and the exposed surface of the

workpiece during a second time period in a series of forward power pulses interspersed with reverse power pulses, to control the deposition of further metal ions over the recessed microstructures relative to the remainder of the surface.

In a still further aspect of the invention, in addition to supplying a forward electroplating power during a first time period and the supplying of a series of forward power pulses interspersed with reverse power pulses during a second time period, reverse electroplating power is supplied for a sustained third period of time, either before or after the second period of time.

The present invention also is directed to the workpieces to which metal structures have been applied in accordance with the processes of the present invention.

In a still further aspect of the present invention, an electroplating apparatus is provided for applying a metal structure to a surface of a workpiece, the workpiece defining a plurality of recessed microstructures. The apparatus includes a reactor for receiving the surface of the workpiece and exposing the surface to an electroplating bath. The electroplating bath includes a source of metal ions and an organic additive that causes the metal ions to be preferentially deposited within the recessed microstructures relative to the remainder of the surface. The apparatus further includes an anode in electrical contact with the electroplating bath, and a power supply for supplying electroplating power between the surface of the workpiece and the anode to electroplate the metal ions onto the surface. The power supply is capable of supplying both forward and reverse power. A controller is included in the apparatus for controlling the power supply, to supply forward electroplating power for a first time period so that the metal ions are deposited on the surface, and for supplying reverse electroplating power for at least a portion of a second time period to control the deposition of further metal ions over the recessed microstructures relative to the remainder of the surface. During the second time period, the provision of electroplating power can be supplied in a sustained fashion, or in a series of reverse power pulses interspersed with forward power pulses.

The present invention thus provides processes and apparatus that enable the use of organic additives or other process conditions for the electrochemical deposition of metal to completely fill recessed micro features in a substrate, while avoiding the development of an overburden of metal above the recessed features relative to the surrounding field area. The present invention results in the

substantial amelioration of such undesirable overburden or bumps being formed, and inhibits or substantially reduces post-plating "momentum" buildup of overburden bumps over the recessed features.

Brief Description of the Drawings

The foregoing aspects and many of the attendant advantages of this invention will become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURES 1a and 1b provide schematic illustrations of the surface of a substrate on which metal has been electrochemically deposited;

FIGURE 2 illustrates SEM cross-sectional views of four substrates including recessed microfeatures of differing sizes conventionally ECD plated with copper using organic additives, and illustrating the overburden bumps formed;

FIGURE 3 provides a series of SEM cross sections of recessed vias illustrating bottom-up plating using ECD copper plating solutions including organic additives;

FIGURE 4 provides a series of SEM cross sections illustrating bottom-up plating and bump formation in a series of recessed trenches, using ECD copper plating solutions including organic additives;

FIGURE 5 provides a graphical representation of the bump heights formed using conventional ECD copper plating solutions including organic additives to fill trenches of various dimensions and pitch;

FIGURES 6a and 6b provide schematic representations of the adsorption of organic additives onto a metal layer being deposited on a substrate including a recessed feature;

FIGURES 7a through 7d provide FIB cross-sectional views of ECD copper overburden formed over recessed features using conventional ECD copper plating solutions including organic additives, for various feature sizes, in which the plating bath did not include leveling agents (FIGURES 7a and 7b) and the same plating baths that included leveling agents (FIGURES 7c and 7d);

FIGURES 8a through 8d illustrate FIB cross-sectional views of the overburden formed over recessed microstructures using reverse current pulsing (Pulsing Schedule PR2, described below) in accordance with a preferred embodiment of the present invention, for features of various sizes and using

plating baths and conditions that otherwise correspond to those used to produce the plated substrates illustrated in FIGURE 2;

FIGURE 9 provides FIB cross sections illustrating bump formation over recessed features in an ECD copper sulfate bath including organic additives, without the use of reverse power, illustrating the differences in bump formation at the edge (top view) and center (bottom view) of a semiconductor wafer;

FIGURE 10 provides a schematic block diagram representation of an apparatus constructed in accordance with the present invention suitable for carrying out the processes in the present invention;

FIGURE 11 provides a longitudinal cross-sectional view of a plating reactor suitable for use in the apparatus of FIGURE 10;

FIGURE 12 provides a graphical representation illustrating bump heights formed as a result of line width and pitch utilizing different plating process parameters in accordance with the present invention;

FIGURE 13 provides a graphical representation of the average bump height in angstroms relative to different plating process parameters in accordance with the present invention;

FIGURE 14 provides FIB cross-sectional views of the plating bump formed above recessed features using a base line set of process parameters without current reversal;

FIGURES 15, 16, and 17 provide FIB cross-sectional views of the plating bumps formed above recessed features using different reverse plating power parameters in accordance with the present invention;

FIGURES 18 and 19 provide FIB cross-sectional views of the plating bumps formed over recessed trenches of various dimensions, with each figure illustrating use of a substrate labeled as: P1, corresponding to the baseline conditions illustrated in FIGURE 14; P2, corresponding to the process parameters in accordance with the present invention illustrated in FIGURE 15; and P3, corresponding to the process parameters in accordance with the present invention illustrated in FIGURE 17;

FIGURE 20 provides a graphical representation of bump height for various trench and pitch dimensions using plating process conditions P1, P2 and P3 as described above for FIGURES 18 and 19; and

FIGURES 21, 22, 23, 24, and 25 illustrate FIB cross-sections of plating bumps formed of recessed features in accordance with various process parameters of the present invention.

Detailed Description of the Preferred Embodiment

The present invention provides processes and methods for electrochemical deposition of metals onto workpieces including recessed microstructures, using plating baths including organic additives and/or process conditions which result in preferential deposition of the metal within the recessed microstructures relative to the surrounding field surface. The present invention provides methods and apparatus for controlling or limiting the build up of an over-burden bump of deposited metal above the recessed microstructure relative to the metal deposited on the surrounding field area.

Specific examples set forth herein below are directed to the electrochemical deposition of copper onto semiconductor wafer substrates. However, it should be understood that the present invention is also suitable for use in depositing other types of metals that may be electroplated onto substrates under conditions that result in preferential deposition of metal within recessed microstructures, in particular sub-micron recessed features, due to the inclusion of organic additives within the electroplating bath that are adsorbed onto the substrate. It is theorized that metals susceptible to processes of the present invention may include copper alloys, e.g., copper zinc, nickel, zinc, and potentially other metals such as chromium, tin, gold, silver, lead, cadmium, platinum, palladium, iridium, ruthenium and various solder compositions, by way of nonlimiting example.

The substrates that are plated in the examples of the present invention set forth herein are semiconductor wafers used in the manufacture of integrated chips. Copper is deposited onto a prepared, patterned water as the substrate. Typically, in the case of copper, the substrate will have been prepared by deposition of a barrier layer and then a metallic seed layer. However, other semiconductor substrates that are prepared such that copper will plate the substrate during an electrochemical deposition are also within the present invention. Further, substrates other than semiconductor wafers are also within the present invention, including micromechanical devices that include recessed microfeatures.

The metal that is to be plated onto the workpieces in accordance with the present invention is present in a plating solution as the primary species of metal

ions to be deposited on the workpiece. Metal ions are deposited under process conditions that preferentially deposit metal ions within the recessed features relative to the surrounding field surface, so as to insure complete fill of the recessed features. Such solutions typically include organic additives that either encourage deposition within the recessed features (i.e., accelerators), or that suppress deposition of metal ions onto the surrounding field surface (i.e., suppressors). As used herein, the term organic additives is intended to encompass accelerators, also known as brighteners or enhancers; suppressors; and also levelers.

Accelerators, also referred to herein as accelerator agents, are typically small molecules which are believed to be adsorbed within the interior of recessed features (without being limited by theory), to accelerate the deposition of metal ions locally within the feature. Suitable accelerators for use in the solutions of the present invention include water soluble salts of organic acids including mercapto or thiol functional groups, as well as other compounds that include the chemical structure S-R_1-S, wherein R_1 is an alkyl or aryl moiety. Such accelerators which are suitable for use in the present invention include those disclosed in U.S. Patent Nos. 5,223,118 to Sonnenberg et al., 4,673,469 to Beach et al., 4,555,315 to Barbieri et al., 4,376,685 to Watson, and 3,770,598 to Creutz, the disclosures of which are hereby expressly incorporated by reference.

The term organic additives also includes suppressor agents, which are typically large molecules that adsorb preferentially to the substrate surface in the field area relative to the recessed features, and that are less adsorbed within the recessed features. Suitable examples of suppressors include polyethylene glycols and polyoxyethylene glycols having molecular weights of approximately 3000-8000. Suitable suppressor agents are commercially available from Shipley Company Inc., Newton, Massachusetts; Enthone-OMI, New Haven, Connecticut; Technic; MacDermit; and Altotech.

The term organic additives as used herein also includes levelers or leveling agents, which are introduced into the plating solution to result in a higher degree of planarization of an electrochemically deposited metal, and in particular are often used in conjunction with suppressors and/or accelerators to counteract to an extent the tendency to build up overburdens over the recessed features. Such levelers include compounds including the chemical structure N-R_1-S, wherein R_1 is an alkyl or aryl group, such as are disclosed in U.S. Patent Nos. 5,223,118,

4,555,315, 4,376,685, and 3,770,598. Other examples of suitable levelers for use in the present invention include those disclosed in U.S. Patent No. 6,024,857 to Reid, the disclosure of which is hereby expressly incorporated by reference, including: polyacrylic acid, polystyrene, polyvinyl alcohol, polyvinyl pyrrolidone, poly(methyl methacrylate), poly(ethylene oxide), poly(dimethylsiloxane) and derivatives, polyacrylamide-co-acrylic acid, poly(2-hydroxyethyl methacrylate), poly(sodium 4-styrene sulfonate) and maleic acid copolymers.

A. ECD Process

The present invention provides process plating parameters, also referred to herein as recipes, that are used to either eliminate, limit or control the formation of momentum plating overburden bumps over recessed features during ECD of a metal onto a substrate. The plating process parameters include the application of a reverse plating power between the surface of a substrate that is received within an electroplating bath and an anode that is also in electrical contact with the electroplating bath. As used herein, the term "reverse power" is used to refer to the application of a reverse current, that would have a tendency if continued to strip metal ions from the substrate, while the term "forward power" is used to refer to the application of a forward current between the anode and the substrate to cause metal ions to be deposited from the plating bath and/or anode onto the substrate.

In a preferred embodiment of the present invention, the plating recipe includes the application of a net forward plating power during a first time period, at a level which causes the deposition of metal onto the substrate and within the recessed features, with the metal being preferentially deposited within the recessed features due to the presence of organic additives in the electroplating bath. Plating process parameters during this first time period are conventional and well known in the art. For example, forward plating power is suitably applied at a level of 1.0 amps for 30 seconds to deposit approximately 0.035 μ of copper on a 200mm wafer.

This application of forward plating power is then followed by application of reverse plating power using a selected waveform, at a level and for a sufficient second period of time so as to limit, and preferentially substantially reduce or eliminate, the formation of an overburden plating bump over the recessed feature.

The formation of an overburden plating bump is prevented from forming during subsequent electroplating and after electroplating is complete.

While not wishing to be limited by theory, it is believed that the reverse plating power should be applied with a sufficient absolute magnitude of reverse current, for a sufficient period of time, so as to substantially desorb the organic additives from the deposited metal on the substrate. After plating is complete in accordance with the process of the present invention, the phenomenon of continued "momentum" plating or build-up of bumps over the recess features is substantially eliminated.

In a preferred embodiment of the present invention, the reverse plating power is supplied during the second time period in a pulsed fashion, including a series of short reverse pulses interspersed with forward reverse pulses. The duration of each reverse pulse is preferably greater than or equal to one millisecond, more preferably greater than or equal to 10 milliseconds, and most preferably as 25 milliseconds. The forward pulses that are interspersed between the reverse pulses are preferably equal to or greater than the duration of the reverse pulses, more preferably are greater than reverse pulses, and most preferably are approximately 60 milliseconds or longer in length. In a further aspect of the present invention, the pulsed application of the reverse plating power is carried out with short breaks in application of current in between the reverse and forward pulses. The absolute magnitude of the reverse pulses will vary depending on the ability to desorb the organic additives, but is preferably equal or greater to 0.05 volts.

One suitable pulsed reverse power sequence for use during the second time period of the present invention, referred to herein as a "PRS" sequence, includes the application of (a) forward plating power at 6-12 amps for 50-150 milliseconds, followed by (b) 0-20 milliseconds of off power, followed by (c) 10 to 50 milliseconds of reverse power at 2 to 10 amps, followed by (d) 0-20 milliseconds of off power. This PRS sequence is repeated multiple times until the total time period desired for application of pulsed reverse power is achieved. The total time period for application of pulsed reverse power is preferably greater than or equal to 10 seconds, more preferably greater than 60 seconds, most preferably at 70-74 seconds.

In lieu of the application or in addition to the application of pulsed reverse power, the present invention also encompasses the application of reverse plating

power in a sustained fashion for a predetermined second period of time. Preferably sustained, steady reverse power is applied in this fashion for greater than or equal to five seconds, most preferably for 10-20 seconds. The absolute magnitude of the sustained reverse power will vary depending on the ability to desorb the organic additives, but preferably is at least 0.05 volts.

The application of a sustained reverse power alone to limit the development of momentum plating appears feasible with control of other plating parameters, and is believed to be potentially workable. However, it is strongly preferred that a pulsed reverse power sequence (such as PRS, for example) be applied during the second time period, either alone, or in conjunction with a sustained reverse power application applied during a third time period either before or after the application of pulsed reverse power.

The preferred embodiments of the present application thus utilize initial net forward plating power to initiate deposition and at least partially fill the recessed microfeatures followed by: (a) the application of pulsed reverse power; (b) the application of net sustained reverse power followed by the application of pulsed reverse power, optionally with the application of forward plating power therebetween; (c) the application of pulsed reverse power followed by the application of sustained reverse power, optionally with the application of forward plating power therebetween; and (d) combinations of the above with single or multiple applications of pulsed reverse power and/or sustained net reverse power. Each period of forward power application may be predominantly forward, with short applications of reverse power application, and visa versa.

While the term "first time period" is used for initial forward plating power application, this may actually include applications of power in multiple time periods at multiple levels. The same alternative arrangements apply for other time periods set forth herein.

The application of reverse power, preferably in a pulsed fashion and potentially augmented with application of reverse power in a sustained fashion, may be used alone to ameliorate the effect of organic additives in producing momentum plating, or may be used in conjunction with other techniques known or developed in the future for amelioration of momentum plating bumps. Thus, for example, the application of reverse power may be used in conjunction with the incorporation of leveler agents into the plating bath. Additionally, it has been found that removal of an ECD plated substrate from a plating bath, followed by

rinsing and immediate heating of the substrate surface to an elevated temperature, such as 100° C or higher, is effective in reducing or eliminating the formation of momentum plating bumps. Such techniques are disclosed in Richard et al., *Roles of Additives During Filling Process of Damascene Structures With Electrochemically Deposited Copper*, pp. 149-153, Advanced Metallization Conference, 1999, MRS, 2/2000. While it is most preferred to avoid this additional processing step through use of the present invention, the present invention encompasses the use of the application of reverse power in conjunction with elevated heating to control or eliminate momentum plating bumps.

The process of the present invention is preferably utilized to prevent the development of an overburden bump. Thus, in a preferred aspect of the present invention, net forward plating power is applied to nominally fill the recessed features, and then reverse plating power is applied, preferably in a pulsed fashion, to desorb the organic additives or otherwise prevent the formation of subsequent momentum plating bumps through other mechanisms. Alternately, the reverse plating power application may be made after an initial forward plating power application which partially fills the recessed features, with additional forward plating power being applied after the application of the reverse plating power to complete the fill of the recessed features. In a preferred aspect of the present invention, forward plating power is initially applied at a low current level, followed by application of a pulsed reverse plating power sequence, followed by application of forward plating power for a third period of time at a current level which is higher than that applied in the first period of time to complete fill of a recessed features. One suitable recipe for application of power in this fashion is set forth in Table I. The reference to PR2 is to the following reverse/forward pulse sequences: (a) 9.0 amps forward power for 95 milliseconds, followed by (b) 5 milliseconds of off power, and then (c) 25 milliseconds reversepower at 4.6 amps, followed by (d) 5 milliseconds of off power.

Table I: Reverse Pulse Recipe

Step	Current	Ampmin	Time
1	1.0 A	.5	30 sec.
2	PR2	7.0	74 sec.
3	6.0 A	7.0	70 sec.

In practice, once a bump has formed it is very difficult to eliminate. It is possible to further optimize the bump reduction recipe by changing the waveform of the PR (pulse reverse) step, the length of the PR step and/or injecting short reverse current steps into the plating recipe. The preferred current pulse reverse step (PR2) used for bump reduction may be improved by either modifying the current levels or the timing. An initial low current step is preferred to maintain good fill, and a final high current DC plating step helps to smooth the surface of the deposited copper, but the invention is not so limited. Moreover, by changing the length of the PR2 in accordance with the disclosure contained herein, it may be possible to reduce the bump size for specific features.

A further example of a preferred plating recipe using the pulsed reverse sequence PR2 is set forth in Table II. FIGURES 8A-8D illustrate the reduction of momentum plating bumps in accordance with this preferred recipe, using a plating bath and conditions that are otherwise the same as those illustrated in FIGURE 2, for various dimensioned trenches.

Table II. Alternate Reverse Pulse Recipe

Step	Current	Ampmin	RPM	Time
1	1.0 A	0.08	75	5 sec
2	1.0 A	0.40	40	25 sec
3	PR2	7.25	40	72 sec
4	6.0 A	7.25	40	72 sec

Another preferred recipe for use in the present invention set forth in Table III, and provides a recipe optimized for electroplating copper from a copper sulfate bath onto a 200mm wafer, to a deposited conformal copper thickness of 1.0 μm at a plating rate of 3400 AMP/mm.

Table III: Alternate Pulse Reverse Recipe

Step	Time	Amp-min	Current
1	0.05 sec.	0.08	1.0A
2	0.25 sec.	0.42	1.0A
3	1.14 sec.	7.0	PR2
4	1.10 sec.	7.0	6.0A

The process recipe of Table III has been used by the inventors to yield a wafer having a plating uniformity cross wafer of 3σ, less than or equal to 6% average, and a wafer to wafer plating uniformity of 3σ, less than or equal to 3% average. Void free fills were experienced, in gaps of less than or equal to 0.25 μm depth and, less than or equal to 1.2μm depth, with a 4:1 aspect ratio. The resulting copper film was found to have a specific resistivity of less than or equal to 1.80μ ohm.cm. Fill impurities were less than or equal to 150 ppms total.

B. Plating Bath Solutions

The above process parameters of Table III were developed for use with a preferred plating bath solution as set forth in Table IV. This aqueous solution includes a source of metal ions in the form of copper sulfate, an acid in the form of sulfuric acid, and a source of chloride in the form of hydrogen chloride. Additionally, organic additives are included to ensure fill of recess features, in the form of both suppressors and accelerators. Suppressors added are available from Shipley Company Inc. of Newton, Massachusetts, under part identifier C-2001, while the accelerators are available from Shipley under part number identifier Solution B-2001, Enthone-OMI, and others.

Table IV: Suitable Plating Bath Solution

	Plating Bath Composition	Operating Range
$CuSO_4*5H_20$	70 g/l(Cu: 17.5 g/l)	50-100 g/l
H_2SO_4	175 g/l	100-275 g/l
HCl	50 ppm	25-100 ppm
Shipley Nanoplate Suppressor Solution C-2001	25 ml/1	5-50 m1/1
Shipley Nanoplate Additive Solution B-2001	3.0 ml/1	0.5-6.0 ml/1

The above representative solution, however, is not intended to limit the use of the present invention. Solutions useful in the present invention include a metal source, which preferably is a source of copper, most preferably copper sulfate. However, other sources of copper are within the scope of the present invention, such as copper gluconate, sodium copper cyanide, copper sulfonate, copper chloride, copper citrate, copper fluoroborate or copper pyrophosphate. Likewise, while sulfuric acid is utilized to yield an acidic bath, other acids such as methyl sulfonic acid, fluoroboric acid, pyrophosphate and citric acid are within the scope of the present invention, and the present invention may also be suitably adapted for use with alkaline plating baths such as those disclosed in International PCT Application No. WO 99/47731 (PCT/US99/06306), the disclosure of which is hereby expressly incorporated by reference. Additionally, other chloride sources may be utilized, and other organic additives may be utilized in lieu of the additives present in the above plating bath solution, such as those disclosed herein above, and ethylene diamine tetra acetic acid (EDTA). Still other plating solution

compositions suitably adapted for use in the present invention, are disclosed in International Patent Application PCT/US00/00155, the disclosure of which is hereby expressly incorporated by reference. The above solutions are in a suitable solvent, and are typically aqueous.

C. ECD Apparatus

The present invention may be suitably carried out in commercially available electroplating apparatus, which are arranged and have controllers that are then modified to be programmed in accordance with the present invention. One suitable electroplating apparatus for use in the present invention is the LT210™ ECD system available from Kalispell, Montana, and as further described in International PCT Application No. WO 98/02911 (PCT/US97/12332), the disclosure of which is hereby expressly incorporated by reference. Other commercially available ECD systems such as the Equinox™ model plating tool, available from Semitool, Inc., are also suitable for use in practicing the present invention.

A schematic representation of one suitable plating system 40 for use in the present invention is provided in FIGURE 10. The plating system 40 includes a plurality of plating apparatus or workstations. Workpieces to be plated, such as semiconductor wafers, are initially prepared for ECD processing at one or more pre-processing stations 42. For example, preprocessing may entail deposition of a barrier layer (e.g., titanium nitride or tantalum nitride), followed by deposition of a seed layer of metal on the barrier layer, such as by physical vapor deposition or alternately chemical vapor deposition. This seed layer optionally may be an ultra thin seed layer, which is then enhanced at a first ECD station 44, at which additional metal is deposited to provide a conformal seed layer of metal. This enhancement may suitably occur in an alkaline plating bath solution, as disclosed in International Application No. WO 99/47731 (PCT/US99/06306), the disclaimer of which is hereby incorporated by reference.

The workpiece with completed seed layer is then passed to a second ECD station 46, in which one or more of the deposition processes of the present invention are carried out. The station 46 includes a reactor, to be described subsequently, in which a surface of the workpiece is received and exposed to a plating bath solution, which is preferably an acidic plating bath solution such as a copper sulfate solution when plating copper, for example. Suitable plating bath solutions are described herein below.

Plating power is supplied to the ECD station 46 by a power supply 48 in accordance with the power schedules and recipes described herein above. (Power supply 48 may also supply power to other stations, or multiple power supplies may be utilized.) This power supply 48 connects electrically between the surface of the workpiece and an anode that is included within the ECD station 46, and that is in contact with the electroplating bath. The power supply 48 is capable of selectively supplying either a forward plating power or a reverse plating power, with both forward and reverse voltage and current control capabilities. The supply of forward and reverse plating power to the reactor within the ECD station 46 is preferentially automatically controlled by a programmable controller 50, which includes a central processing unit that operates in accordance with program code to cause the power supply 48 to supply forward, reverse or no power, at desired levels and for desired time periods in accordance with the present invention. The controller 50 includes a data input device (not shown), such as a keypad, touch screen, other user interface, or a floppy or CD disk drive. The system 40 also includes a rinse station 52, in which the workpiece from the ECD station 46 is received and rinsed. The system may also include further stations (not shown) for additional processing steps, as dictated by the workpiece being plated. Passage of the workpiece through the various stations may be automated through the use of a conveyor system (not shown).

The ECD station 46 includes a reactor vessel in which the electroplating bath is held and which receives at least one surface of the workpiece on which the metal is to be deposited. A suitable reactor is disclosed in the aforementioned International Application WO 98/02911.

An alternate reactor vessel, also suitable for use in the present invention, is disclosed in International Application WO 00/03067 (PCT/US99/15430), the disclosure of which is hereby expressly incorporated by reference. One suitable reactor constructed in accordance with WO 00/03067 for use in the processing station 46 of the present invention is illustrated in FIGURE 11. The reactor 60 includes a processing head 62 and an electroplating bowl assembly 64. The electroplating bowl assembly 64 includes a cup assembly 70 that is disposed within a reservoir container 72. The cup assembly 70 includes a fluid chamber 72 portion that holds the electroplating bath fluid. The cup assembly also includes a depending annular skirt 74 which extends below the cup bottom 76, and which includes apertures opening therethrough for fluid communication of the plating

bath solution, and for release of any gasses that might collect as the chamber of the reservoir assembly is filled with plating solution. The cup is preferentially made from a material that is inert to plating solutions, such as polypropylene.

A lower opening in the bottom wall of the cup assembly 70 is connected to a polypropylene (or other material) riser tube 78, which preferably is adjustable in height relative to the cup assembly by a threaded connection. A first end of the riser tube 78 is secured to the rear portion of an anode shield 80, which supports an anode 82. A fluid inlet line 84 is disposed within the riser tube 78. Both the riser tube 78 and the fluid inlet line 84 are secured to the processing bowl assembly 64 by a fitting 86. The fitting 86 can accommodate height adjustment of both the riser tube 78 and the inlet line 84. As such, this connection provides for vertical adjustment of the anode 82 position. The inlet line 84 is preferably made from a conductive material, such as titanium, and is used to conduct electrical current to the anode 82 from the power supply 48, as well as to supply fluid to the cup assembly 70.

Electroplating solution is provided to the cup assembly 70 through the fluid inlet line 84 and proceeds therefrom through a plurality of fluid inlet openings 88. The plating solution then fills the chamber 72 through opening 88, as supplied by a plating fluid pump (not shown) or other suitable supply.

The upper edge of the cup sidewall 90 forms a weir, which limits the level of electroplating solution within the cup. This level is chosen so that only the bottom surface of a wafer W (or other workpiece) is contacted by the electroplating solution. Excess solution pours over this top edge into an overflow chamber 92.

The outflow liquid from the chamber 72 is preferably returned to a suitable reservoir, where it can be treated with additional plating chemicals to adjust the levels of the constituents and then recycled to the plating chamber 72.

In one embodiment of the apparatus for electroplating, the anode 82 is a consumable anode used in connection with the plating of copper or other metals onto the workpiece. The specific anode may alternatively be an inert anode, with the anode used in reactor 60 varying depending upon the specifics of the plating liquid and process being used.

The embodiment illustrated in FIGURE 11 also employs a diffuser plate 93 that is disposed above the anode 82, providing an even distribution of the flow of fluid across the surface of the wafer W. Fluid passages are provided over

all or a portion of the diffuser plate 93, to allow fluid communication therethrough. The height of the diffuser plate within the cup assembly may be adjustable by using a height adjustment mechanism 94.

The anode shield 80 is secured to the underside of the anode 82 using anode shield fasteners 96, to prevent direct impingement by the plating solution as the solution passes into the processing chamber 72. The anode shield 80 and anode shield fasteners 96 are preferably made from a dielectric material, such as polyvinylidene fluoride or polypropylene. The anode shield serves to electrically isolate and physically protect the backside of the anode.

The processing head 62 holds a wafer W (or other workpiece) within the upper region of the processing chamber 72. In a preferred embodiment, the head 62 is constructed to rotate the wafer W within the chamber 72 about on axis R. To this end, the processing head 62 includes a rotor assembly 98 having a plurality of wafer engaging contact fingers 100 that hold the wafer against features of the rotor. The fingers 100 are preferably adapted to conduct current between the wafer and the electrical power supply 48.

The processing head 62 is supported by a head operator (not shown) that is adjustable to adjust the height of the processing head. The head operator also has a head connection shaft 102 that is operable to pivot about a horizontal pivot axis. Pivotal action of the processing head using the operator allows the processing head to be placed in an open or face-up position (not shown) for loading and unloading of the wafer W. FIGURE 11 illustrates the processing head pivoted into a face-down position in preparation for processing. However, this flipping of the wafer is not necessary for carrying out the present invention.

D. Other Process Parameters

Another method of the present invention for modifying the final surface topography is to modify deposition parameters other than or in addition to current density and waveform; such as plating solution fluid flow, and wafer rotation velocity. Although these parameters may be adjusted at any time during the deposition process, it is usually preferred to utilize parameters that have been optimized for feature fill capability and electromigration resistance until the small features are filled, then switch to a set of parameters that are optimized for the minimization of these surface features.

An example of the capability of modifying the surface topography through the use of process parameters while maintaining a consistent bath composition is

seen in FIGURE 9. The data represented in this FIGURE were produced by modifying waveform and current density as described above, and fluid flow, using the same copper plating chemistry as used to produce the wafer illustrated in FIGURE 2. As seen in FIGURE 9, the process parameters investigated had a large effect on the surface topography.

E. Examples

The electrochemical deposition used in the examples that follow was performed in a Semitool ECD reactor, identical to that on an LT210c copper ECD system for copper interconnect manufacturing, and including a power supply having both forward and reverse voltage and current control. All wafers were 200 mm silicon wafers with trench and via features etched in silicon dioxide, and with barrier and copper seed layers deposited over these features to provide electrical conductivity. The copper plating additives used in this study were commercially available and/or experimental additives available from Enthone-OMI, and Shipley Company. Typical acid copper plating solutions as set forth on Table IV, which contain copper sulfate, sulfuric acid and hydrochloric acid, were used for all the examples.

Example I

In a first series of experiments performed to investigate the elimination of bump formation, a profilometer was used to measure bump height over several feature sizes and densities that were plated under different conditions, as set forth in Tables V-XIII, referred to as recipes A-I. The pulse reverse waveforms referenced in the tables are defined in Table XIV. The bump heights produced from each of these recipes A-I are summarized in FIGURES 12 and 13. The data in FIGURE 13 represents the bump height averaged over all the different feature sizes with each plating recipe. FIGURE 12 provides the bump height over each specific feature size and pitch. The bump height is expressed in angstroms above the field as measured with a prolifometer. An extended dwell step after the fill step had only a minimal effect (Recipes H and I). The most effective methods used a PR2 plating step to prevent the formation of bumps as the features are filled (Recipes A, C-F). The PR1 plating step (no data shown) only slightly reduced the bump formation. The addition of short (10 second) reverse current steps during fill also significantly reduced bump formation (Recipes A, C, D, F).

TABLE V: BUMP REDUCTION RECIPE A

Step	Current	Time
1	0.5 A	5 sec
2	4.5 A	30 sec
3	-1.6 A	10 sec
4	4.5 A	30 sec
5	-1.6 A	10 sec
6	PR2	20 sec
7	6.0 A	1:45

TABLE VI: BUMP REDUCTION RECIPE B

Step	Current	Time
1	0.5 A	30 sec
2	PR2	2:15

TABLE VII: BUMP REDUCTION RECIPE C

Step	Current	Time
1	1.0 A	5 sec
2	4.5 A	30 sec
3	-1.6 A	30 sec
4	PR	40 sec
5	6.0 A	2:00

TABLE VIII: BUMP REDUCTION RECIPE D

Step	Current	Time
1	1.0 A	5 sec
2	4.5 A	30 sec
3	-1.6 A	15 sec
4	PR2	20 sec
5	6.0 A	2:00

TABLE IX: BUMP REDUCTION RECIPE E

Step	Current	Time
1	1.0 A	60 sec
2	-1.6 A	15 sec
3	PR2	20 sec
4	6.0 A	2:15

TABLE X: BUMP REDUCTION RECIPE F

Step	Current	Time
1	4.5 A	60 sec
2	-1.5 A	15 sec
3	PR2	20 sec
4	6.0 A	1:20

TABLE XI: BUMP REDUCTION RECIPE G

Step	Current	Time
1	1.0 A	5 sec
2	FP	2:25

TABLE XII: BUMP REDUCTION RECIPE H

Step	Current	Time
1	1.0 A	5 sec
2	4.5 A	15 sec
3	Dwell	1:00
4	6.0 A	2:10

TABLE XIII: BUMP REDUCTION RECIPE I

Step	Current	Time
1	0.5 A	5 sec
2	4.5 A	30 sec
3	Dwell	1:00
4	6.0 A	2:00

Table XIV: Pulse Waveforms

PR1: 20 msec forward/0msec off at 7.35 amps
1 msec reverse/0msec off at 14.7 amps

PR2: 95 msec forward/5 msec off at 9.0 amps
25 msec reverse/5 msec off at 4.6 amps

FP: 95 msec forward/35 msec off at 8.6 amps

Example II

In the second experiment four different recipes were compared using FIB cross sections, and using the same wafers, equipment and chemistry as in Example I. Each recipe is outlined in Tables XV-XVIII, identified as baseline (no reverse current) and Recipes 1-3, respectively. It is noted that Recipe A from Example 1 is the same as Recipe 3 from Example II. The resulting wafers are shown in FIGURES 14, 15, 16, and 17, corresponding to the baseline, Recipe 1, Recipe 2, and Recipe 3, respectively.

In the baseline DC recipe (FIGURE 14) the bumps were much larger than the other recipes (see FIGURES 15-17). The best results were attained with recipe 3 (recipe A). Additional cross sectional views of the wafers resulting from this experiment are shown in FIGURES 18 and 19. Wafers labeled as "P1" in these figures correspond to the baseline recipe; wafers labeled as "P2" correspond to Recipe 1; and wafers labeled as "P3" correspond to recipe 3. FIGURE 20 provides bump heights as a function of feature size for these same three recipes.

TABLE XV: BASELINE RECIPE

Step	Current	Amp-min	RPM	Time
1	1.0 A	0.08	75	5 sec
2	4.5 A	4.4	40	58 sec
3	6.0 A	10	40	100 sec

TABLE XVI: BUMP REDUCTION RECIPE 1

Step	Current	Amp-min	RPM	Time
1	1.0 A	0.08	75	5 sec
2	1.0 A	0.40	40	25 sec
3	PR2	7.25	40	72 sec
4	6.0 A	7.25	40	72 sec

TABLE XVII: BUMP REDUCTION RECIPE 2

Step	Current	Amp-min	RPM	Time
1	0.5 A	0.04	75	5 sec
2	4.5 A	4.5	40	60 sec
3	PR2	7.0	40	70 sec
4	6.0 A	3.0	40	30 sec

TABLE XVIII: BUMP REDUCTION RECIPE 3

Step	Current	Amp-min	RPM	Time
1	.05 A	.04	75	5 sec
2	4.5 A	2.25	40	30 sec
3	-1.6 A	-.27	40	10 sec
4	4.5 A	2.25	40	30 sec
5	-1.6 A	-.27	40	10 sec
6	PR2	2.0	40	20 sec
7	6.0 A	10.5	40	1:45 sec

Example III

In the third experiment, five additional recipes were compared using FIB cross sections, and using the same wafers, equipment and chemistry as in Example I. Each recipe is outlined in Tables XIX-XXIII, identified as wafers 14-18, respectively. Images of the resulting wafers 14-18 are illustrated in FIGURES 21-25, respectively.

TABLE XIX:Wafer 14 Recipe

Step	Current	Amp-min	Time
1	4.5 A	2.25	
2	-1.6 A		15 sec
3	PR2		20 sec
4	6.0 A		2 min

TABLE XX:Wafer 15 Recipe

Step	Current	Amp-min	Time
1	4.5 A	1.0	
2	-1.6 A		5 sec
3	6.0 A		2 min

TABLE XXI:Wafer 16 Recipe

Step	Current	Amp-min	Time
1	4.5 A	2.25	
2	-1.6 A		5 sec
3	6.0 A		2 min

TABLE XXII:Wafer 17 Recipe

Step	Current	Amp-min	Time
1	4.5 A	1.0	
2	dwell		1.0 min
3	6.0 A		2.0 min

TABLE XXIII:Wafer 18 recipe

Step	Current	Amp-min	Time
1	4.5 A	2.25	
2	dwell		1.0 min
3	6.0 A		2.0 min

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A process for depositing a metal structure on a surface of a workpiece defining a plurality of recessed microstructures, comprising:

(a) exposing the surface of the workpiece to an electroplating bath including a source of metal ions to be deposited on the surface and an organic additive that influences the metal ions to be preferentially deposited within the recessed microstructures relative to the surrounding surface;

(b) supplying net forward electroplating power between the exposed surface of the workpiece and an anode disposed in electrical contact with the electroplating bath for a first time period selected so that metal ions are deposited on the surface; and

(c) reversing the electroplating power supplied between the anode and the exposed surface of the workpiece for at least a portion of a second time period selected to control the deposition of further metal ions over the recessed microstructures relative to the surrounding surface.

2. The process of Claim 1, wherein the first time period and a level of forward electroplating power supplied during the first time period are selected such that metal ions are deposited within the recessed microstructures to nominally fill the recessed microstructures during the first time period, and the second time period and a level of reverse electroplating power supplied during the second time period are selected to ameliorate deposition of an overburden of metal ions over the recessed microstructures relative to the remainder of the surface.

3. The process of Claim 1, wherein during the second time period the power that is supplied between the anode and the exposed surface of the workpiece is alternated between pulses of forward power interspersed with pulses of reverse power.

4. The process of Claim 3, wherein the duration of each pulse of reverse power is greater than 1 millisecond.

5. The process of Claim 4, wherein the duration of each pulse of reverse power is greater than or equal to 10 milliseconds.

6. The process of Claim 3, wherein the second time period is greater than or equal to 10 seconds.

7. The process of Claim 6 wherein the second time period is greater than or equal to 60 seconds.

8. The process of Claim 1, wherein the reverse electroplating power is sustained for the duration of the second time period, further comprising supplying electroplating power between the exposed surface of the workpiece and the anode for a third time period before or after the second time period during which third period forward and reverse electroplating power is supplied in a series of interspersed pulses.

9. The process of Claim 8, wherein the second time period during which reverse electroplating power is supplied is greater than or equal to 1 second.

10. The process of Claim 9, wherein the reverse electroplating power is supplied for a second time period of greater than or equal to 5 seconds.

11. The process of Claim 1, wherein the reverse electroplating power is supplied at a reverse current of absolute magnitude greater than 1 amp.

12. The process of Claim 1, wherein the reverse electroplating power is supplied at a voltage potential of absolute magnitude greater than 0.05 volts.

13. The process of Claim 1, wherein the metal that is deposited comprises copper.

14. The process of Claim 13, wherein the source of metal ions comprises copper sulfate.

15. The process of Claim 14, wherein the electroplating bath further comprises a source of chlorine ions.

16. The process of Claim 1, wherein the organic additive comprises an accelerator agent.

17. The process of Claim 16, wherein the accelerator agent includes the chemical structure $S\text{-}R_1\text{-}S$, wherein R_1 comprises an alkyl or an aryl group.

18. The process of Claim 1, wherein the organic additive comprises a suppressor agent.

19. The process of Claim 18, wherein the suppressor agent comprises a compound including the chemical structure $N\text{-}R_1\text{-}S$, wherein R_1 comprises an alkyl or an aryl group.

20. The process of Claim 1, wherein the organic additive comprises a leveler agent.

21. The process of Claim 20, wherein the leveler agent comprises a polyethylene glycol or polyoxyethylene glycol.

22. The process of Claim 1, further comprising supplying forward electroplating power between the surface of the workpiece and the anode for a third time period after the second time period.

23. The product produced by the process of Claim 1.

24. A process for depositing a metal structure on a surface of a workpiece defining a plurality of recessed microstructures, comprising:

(a) exposing the surface of the workpiece to an electroplating bath including a source of metal ions to be deposited on the surface and an organic additive that is absorbed on the surface and influences the metal ions to be preferentially deposited within the recessed microstructures relative to the remainder of the surface;

(b) supplying net forward electroplating power between the exposed surface of the workpiece and an anode disposed in electrical contact with the electroplating bath for a first time period and at a first level of supplied power selected so that metal ions are deposited to nominally fill the recessed microstructures; and

(c) reversing the electroplating power supplied between the anode and the exposed surface of the workpiece during at least a portion of a second time period and at a second level of applied power selected to limit the deposition of further metal ions over the nominally filled recessed microstructures relative to the remainder of the surface to desorb the organic additives to ameliorate the development of an overburden of metal over the recessed microstructures.

25. A process for depositing a metal structure on a surface of a workpiece defining a plurality of recessed microstructures, comprising:

(a) exposing the surface of the workpiece to an electroplating bath including a source of metal ions to be deposited on the surface;

(b) supplying net forward electroplating power between the exposed surface of the workpiece and an anode disposed in electrical contact with the electroplating bath for a first period of time and under a first set of plating process parameters such that metal ions are preferentially deposited within the recessed microstructures relative to the remainder of the surface; and

(c) supplying electroplating power between the anode and the exposed surface of the workpiece during a second time period in a series of forward plating power pulses interspersed with reverse plating power pulses to control the deposition of further metal ions over the recessed microstructures relative to the remainder of the surface.

26. A process for depositing a metal structure on a surface of a workpiece defining a plurality of recessed microstructures, comprising:

(a) exposing the surface of the workpiece to an electroplating bath including a source of copper ions, an acid, a source of chlorine ions and an organic additive that influences the metal ions to be preferentially deposited within the recessed microstructures relative to the remainder of the surface;

(b) supplying net forward electroplating power between the exposed surface of the workpiece and an anode disposed in electrical contact with the electroplating bath for a first period of time and at a first level of supplied power such that metal ions are preferentially deposited within the recessed microstructures relative to the remainder of the surface; and

(c) supplying electroplating power between the anode and the exposed surface of the workpiece during a second time period in a series of forward plating power pulses interspersed with reverse plating power pulses to control the deposition of further metal ions over the recessed microstructures relative to the remainder of the surface.

27. The product produced by the process of Claim 26.

28. An electroplating apparatus for applying a metal structure to a surface of a workpiece defining a plurality of recessed microstructures, comprising:

(a) a reactor for receiving the surface of the workpiece and exposing the surface to an electroplating bath including a source of metal ions and an organic additive that influences the metal ions to be preferentially deposited within the recessed microstructures relative to the remainder of the surface;

(b) an anode in electrical contact with the electroplating bath;

(c) a power supply for supplying electroplating power between the surface of the workpiece and the anode to electroplate the metal ions onto the surface, the power supply being capable of supplying forward power and reverse power; and

(d) a controller for controlling the power supply to supply net forward electroplating power for a first time period so that the metal ions are deposited on the surface and for supplying reverse electroplating power for at least a portion of a second time period to control the deposition of further metal ions over the recessed microstructures relative to the remainder of the surface.

29. The process of Claim 28, wherein during the second time period the power that is supplied between the anode and the exposed surface of the workpiece is alternated between pulses of forward plating power interspersed with pulses of reverse plating power.

30. The process of Claim 28, wherein the controller is operable to control the power supply to supply sustained reverse electroplating power for the duration of the second time period, wherein the controller is further operable to control the power supply to supply electroplating power between the exposed surface of the workpiece and the anode for a third time period during which forward and reverse electroplating power is supplied in a series of interspersed pulses.

31. The process of Claim 1, wherein the controller is operable to control the power supply to supply forward electroplating power between the surface of the workpiece and the anode for a third time period after the second time period.

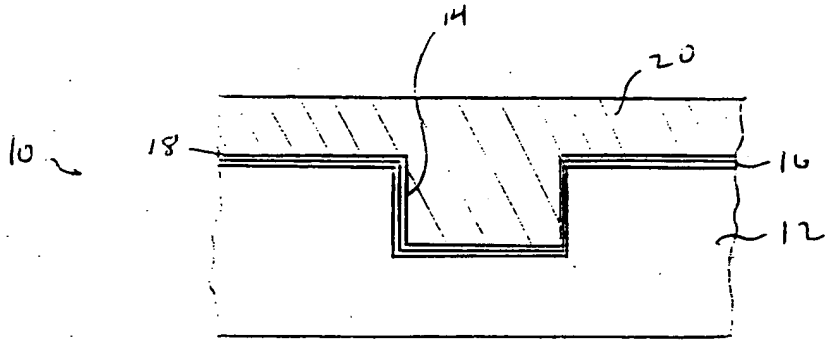

FIG. 1(a)

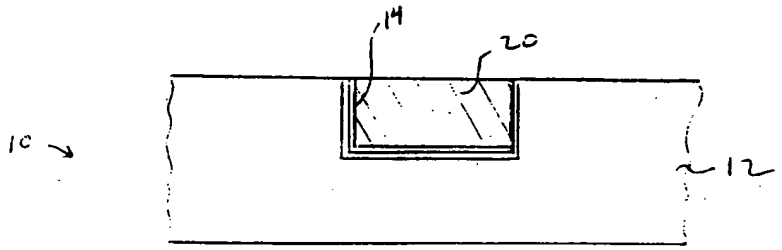

FIG. 1(b)

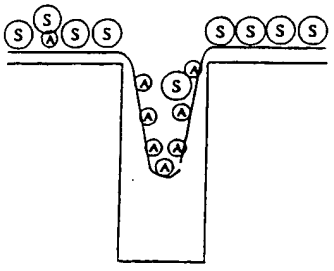

FIG. 6(a)

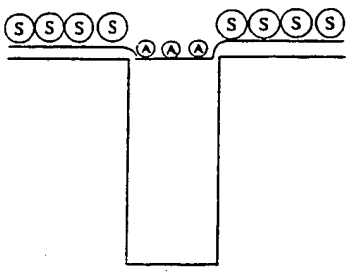

FIG. 6(b)

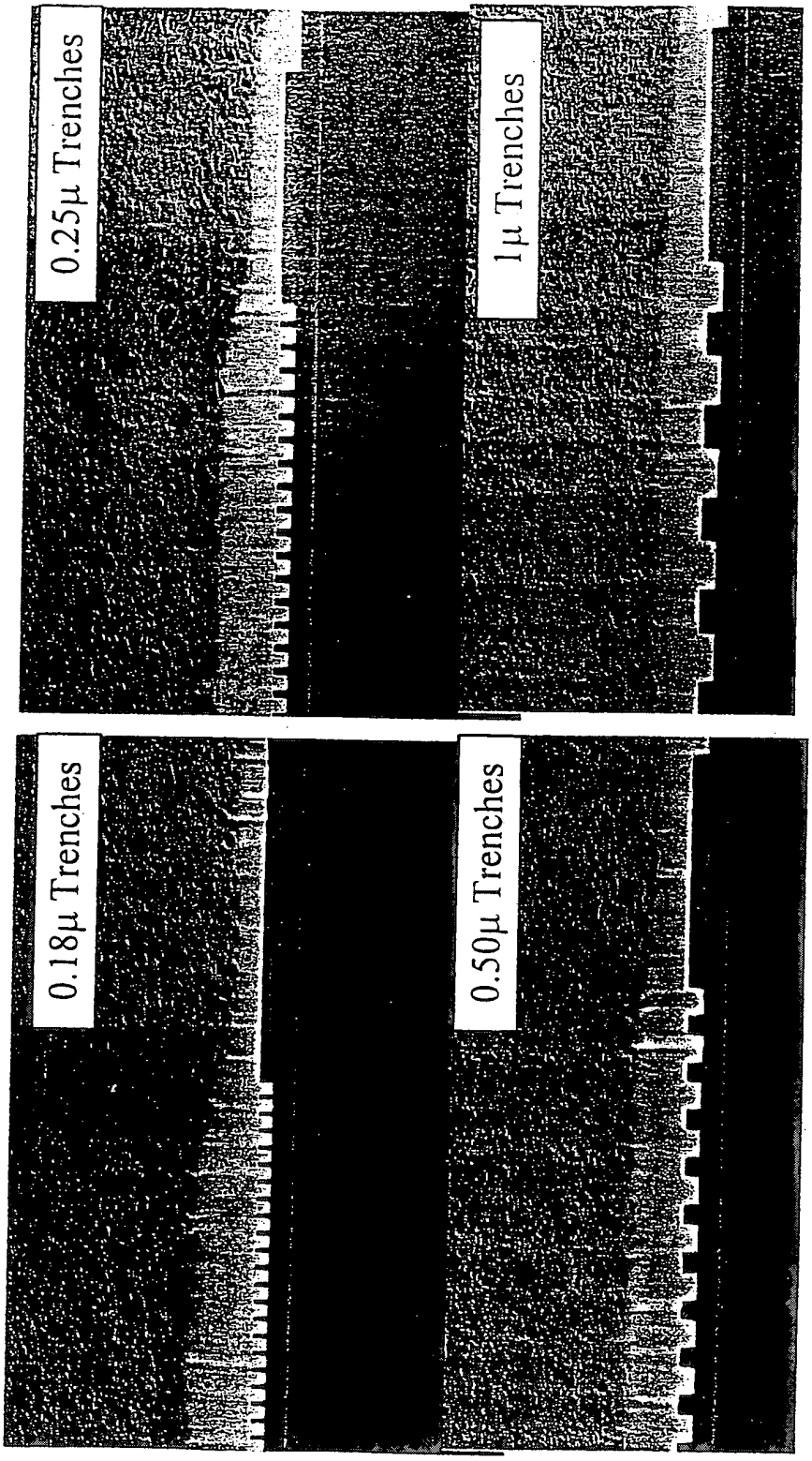

FIG. 2

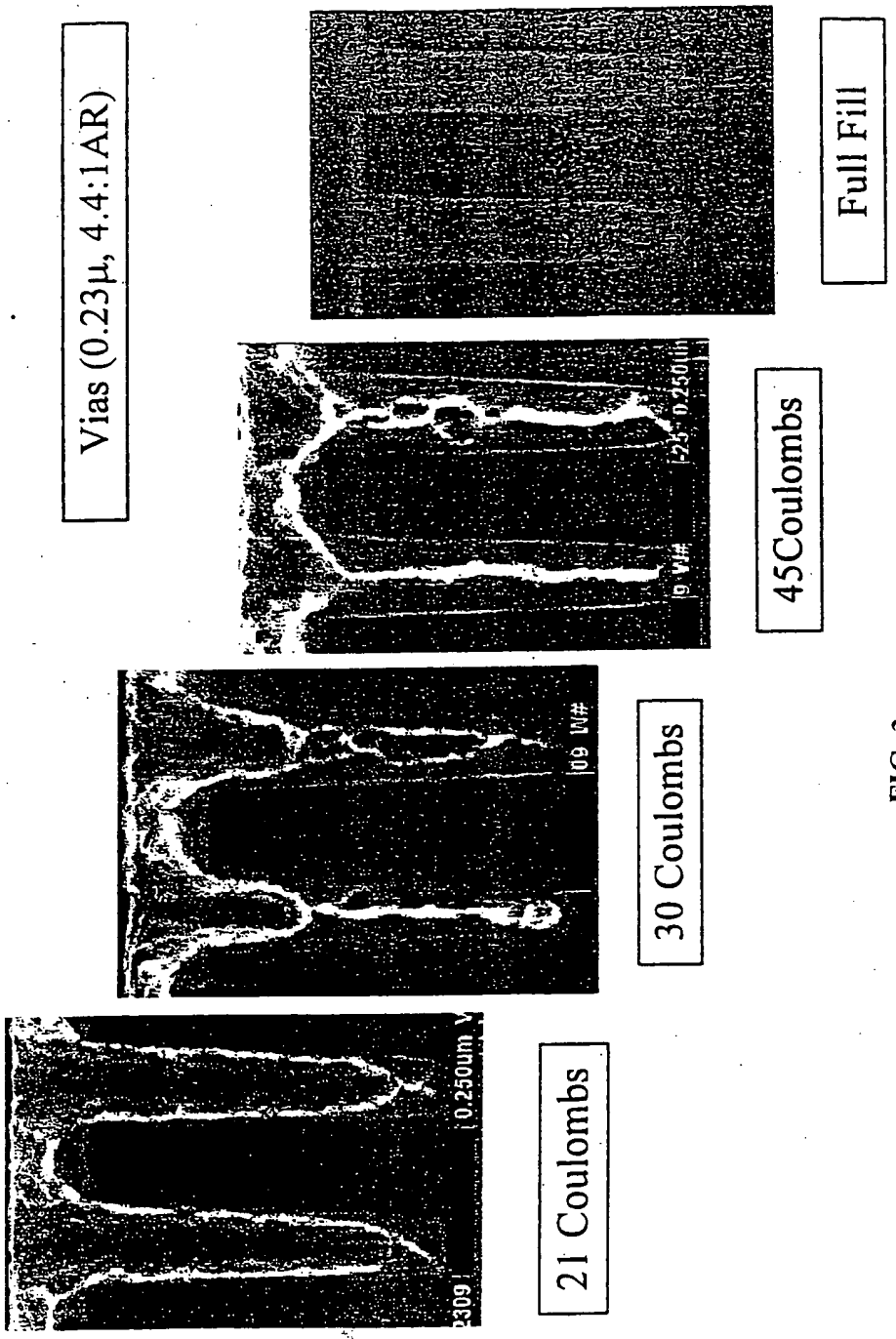
Vias (0.23μ, 4.4:1AR)
21 Coulombs
30 Coulombs
45Coulombs
Full Fill

FIG. 3

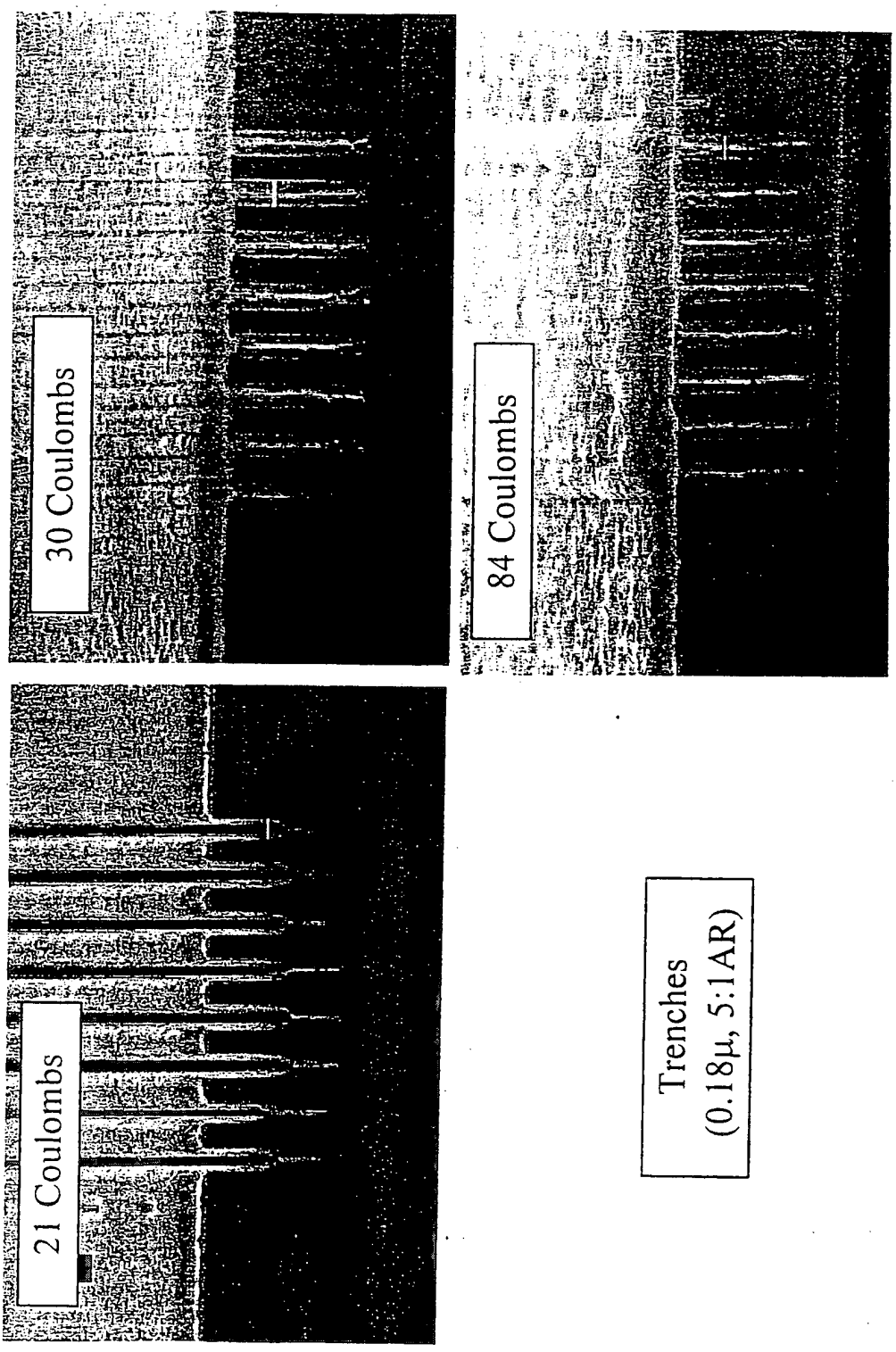

FIG. 4

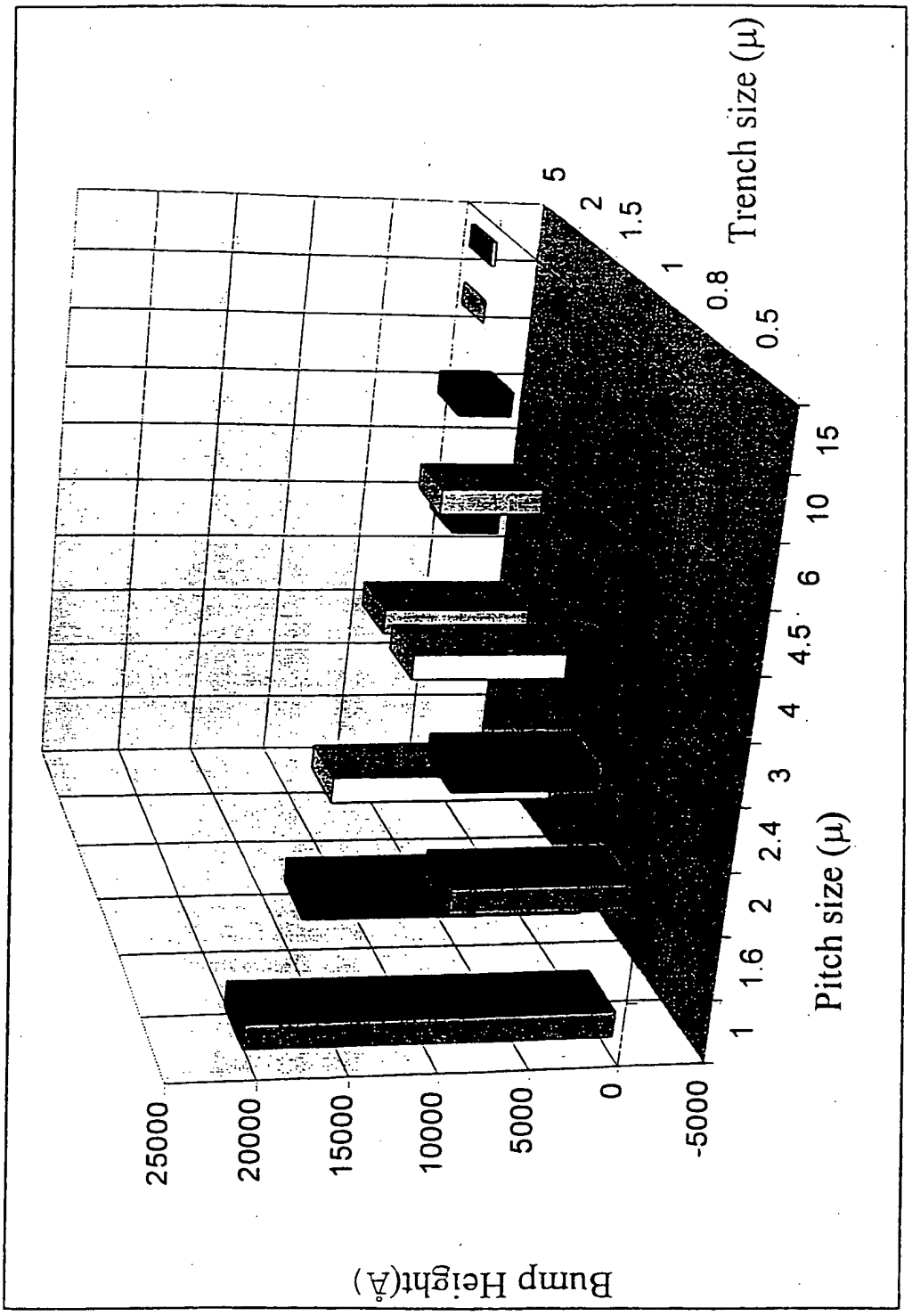
Bump Height(Å)
25000
20000
15000
10000
5000
0
-5000
Pitch size (μ)
1
1.6
2
2.4
3
4
4.5
6
10
15
Trench size (μ)
0.5
0.8
1
1.5
2
5

FIG. 5

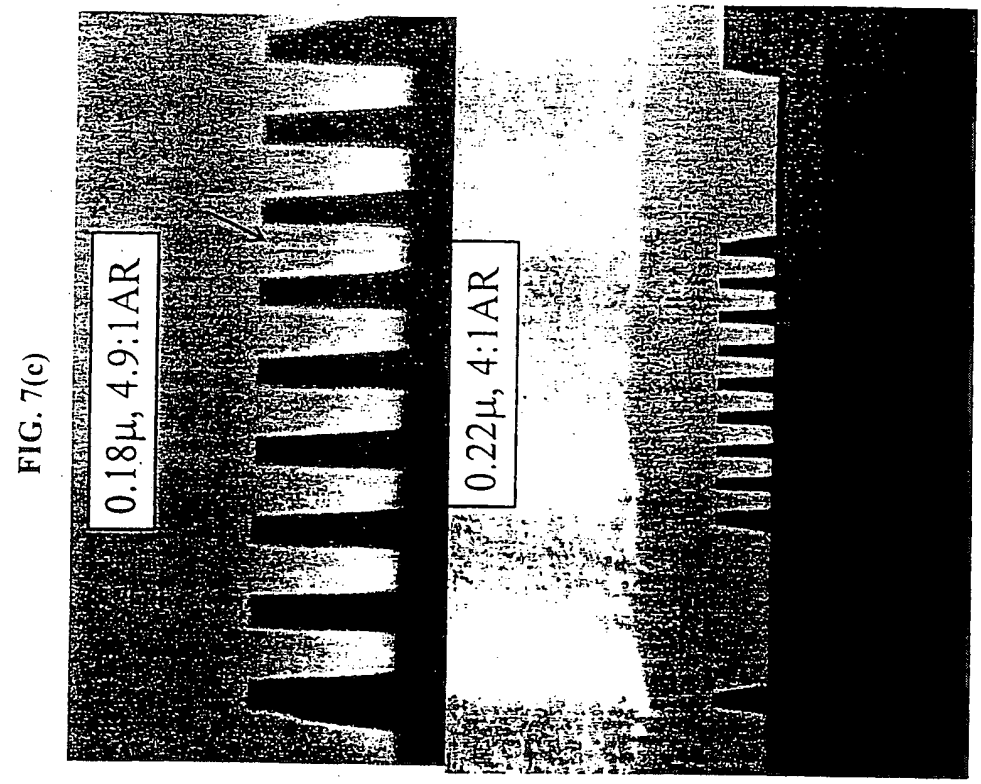

FIG. 7(c)

FIG. 7(d)

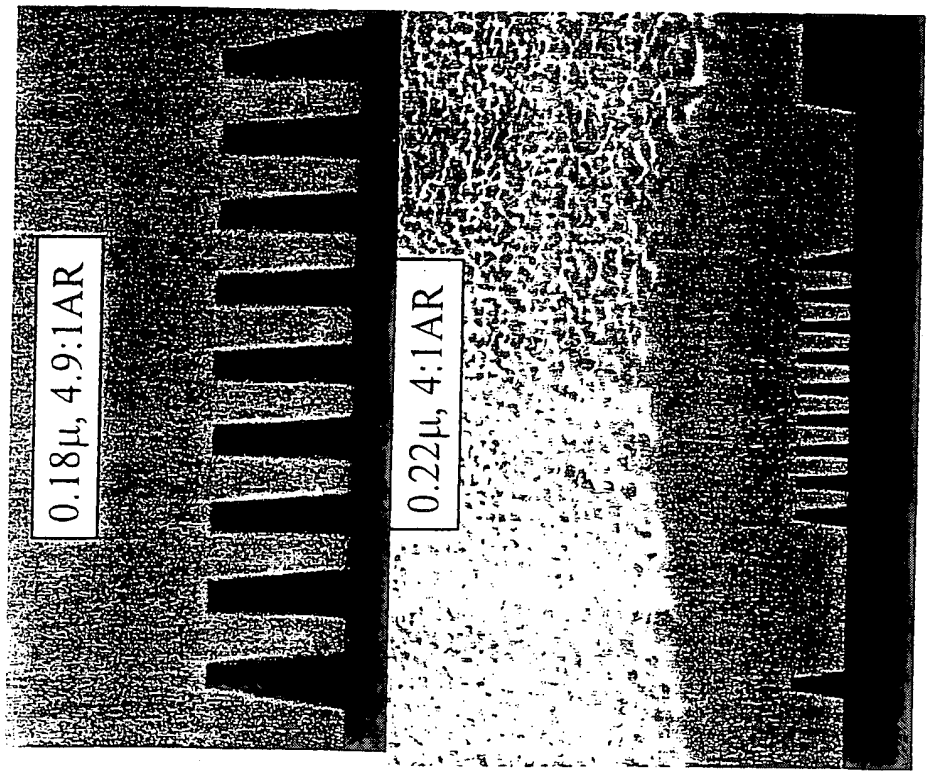

FIG. 7(a)

FIG. 7(b)

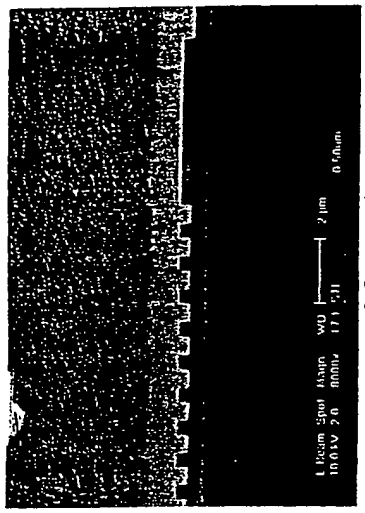

FIG. 8(c) 0.5μ trenches

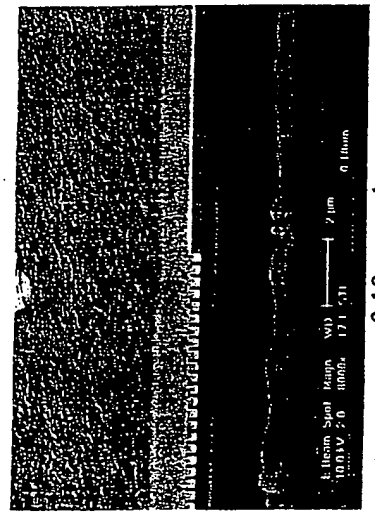

FIG. 8(a) 0.18μ trenches

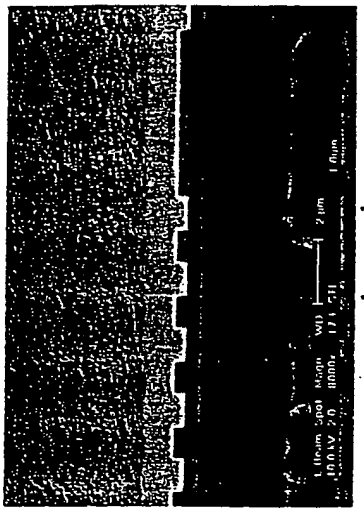

FIG. 8(d) 1μ trenches

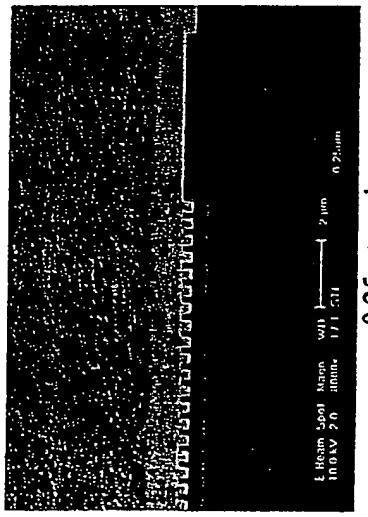

FIG. 8(b) 0.25μ trenches

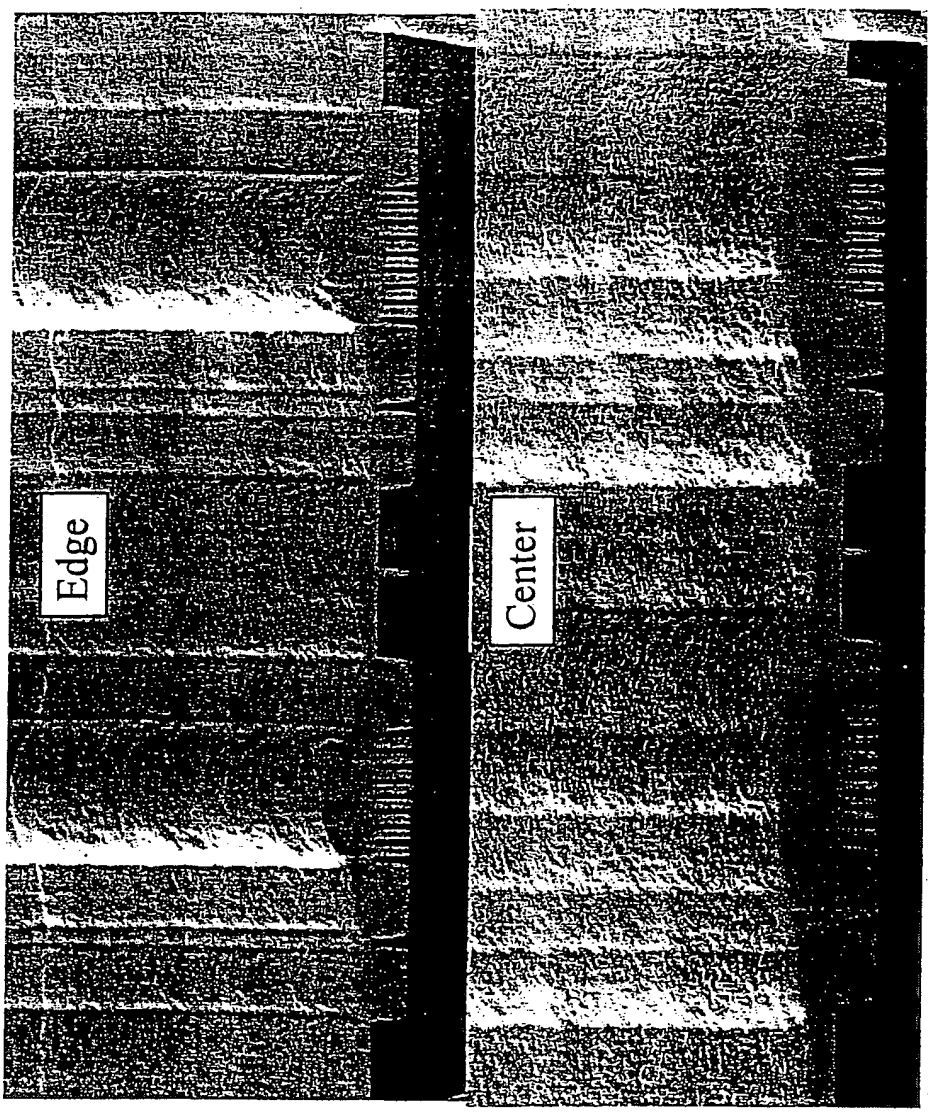

FIG. 9

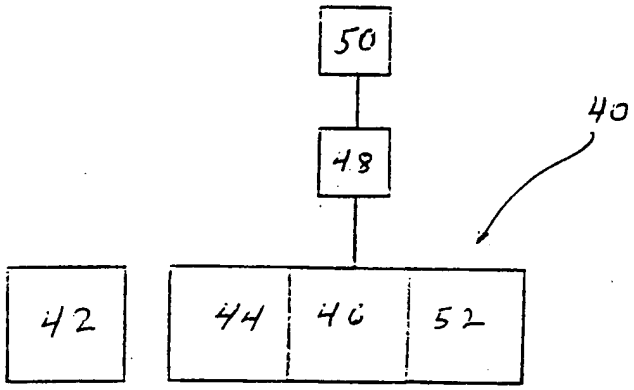

FIG. 10

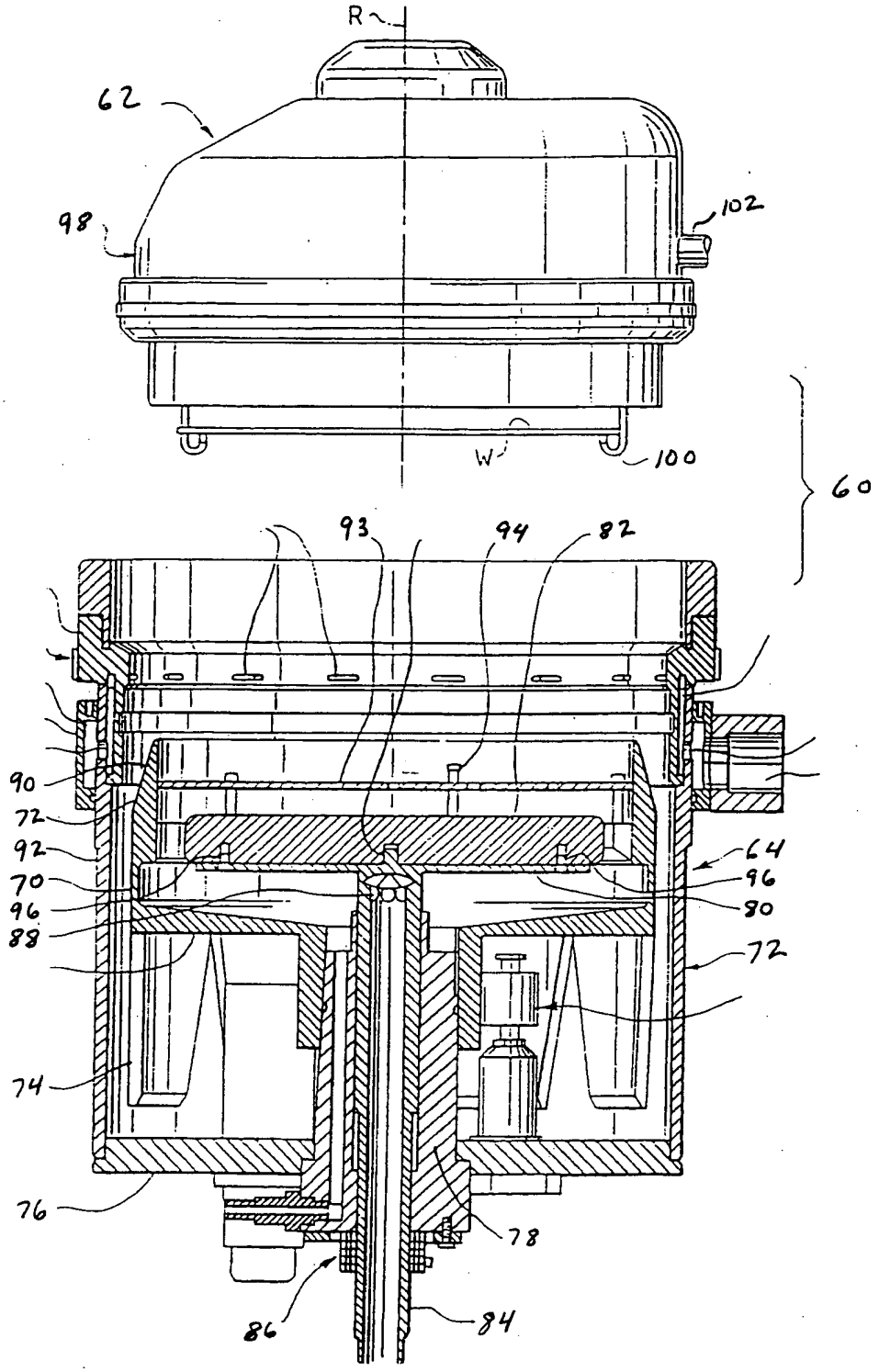
R
62
98
102
W
100
60
93
94
82
90
72
92
70
96
88
64
96
80
72
74
76
78
86
84

FIG. 11

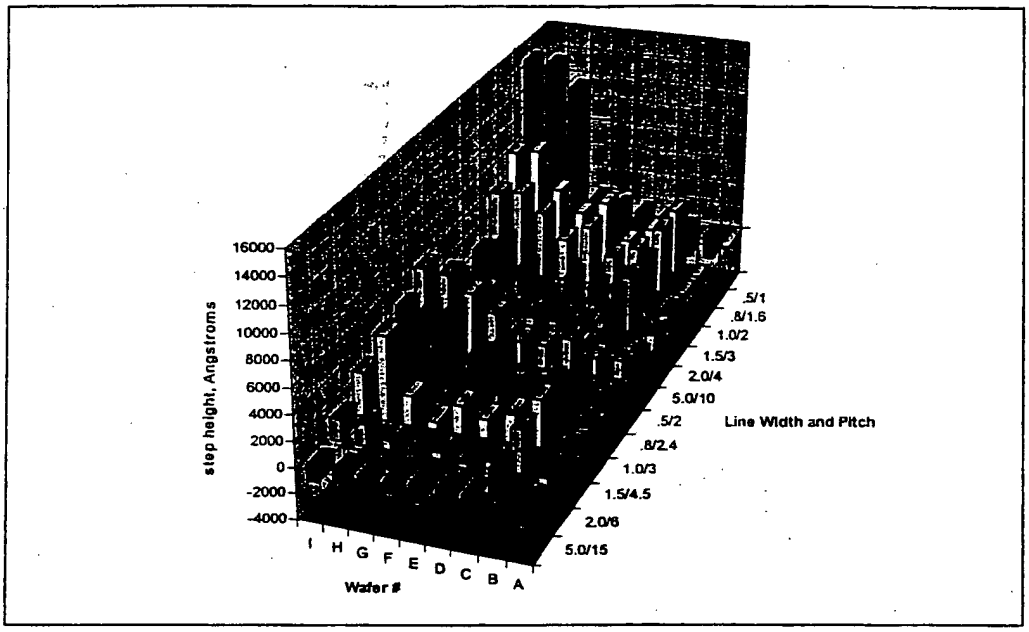
step height, Angstroms
16000
14000
12000
10000
8000
6000
4000
2000
0
-2000
-4000
I H G F E D C B A
Wafer #
.5/1
.8/1.6
1.0/2
1.5/3
2.0/4
5.0/10
.5/2
.8/2.4
1.0/3
1.5/4.5
2.0/6
5.0/15
Line Width and Pitch

FIG. 12

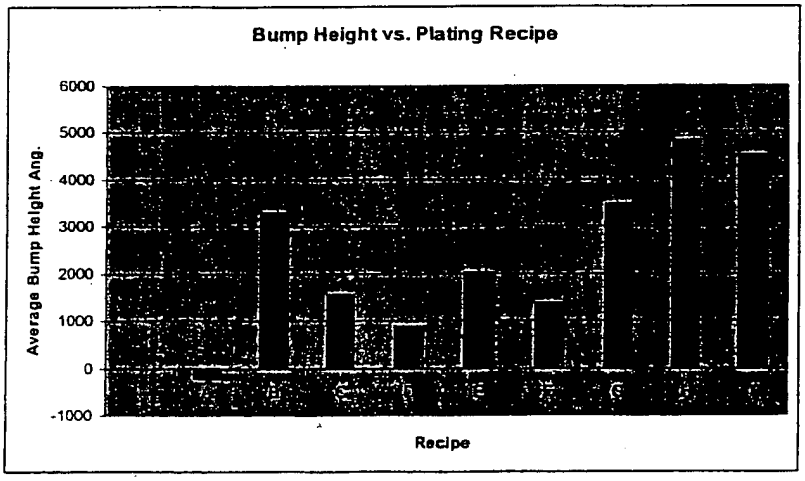
Bump Height vs. Plating Recipe
Average Bump Height Ang.
6000
5000
4000
3000
2000
1000
0
-1000
Recipe

FIG. 13

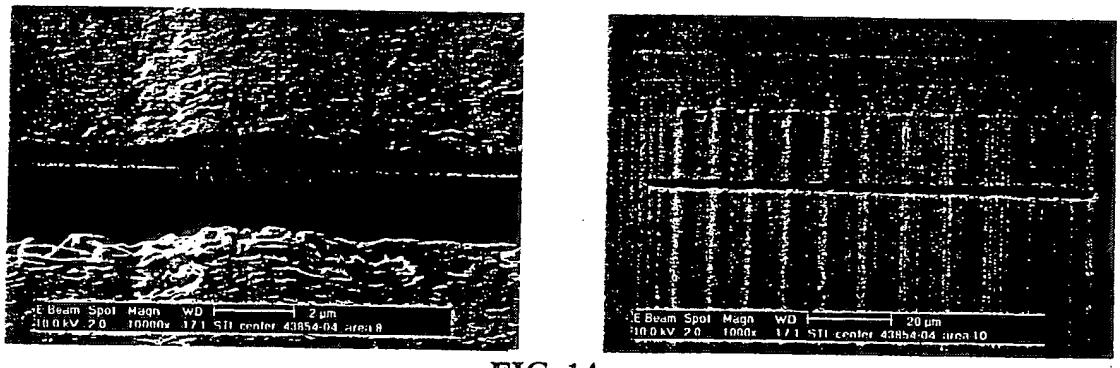

FIG. 14

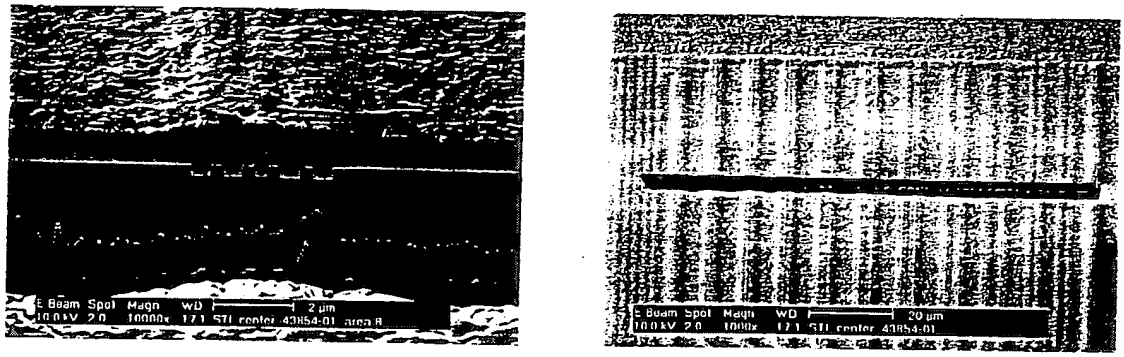

FIG. 15

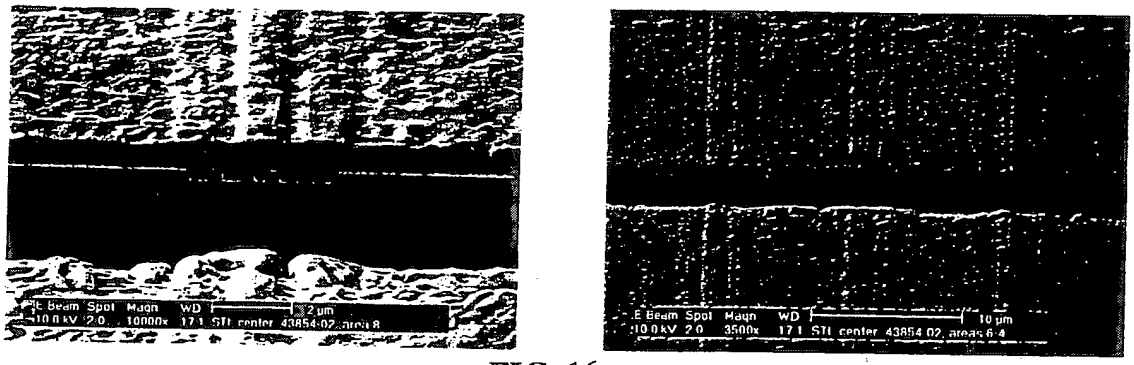

FIG. 16

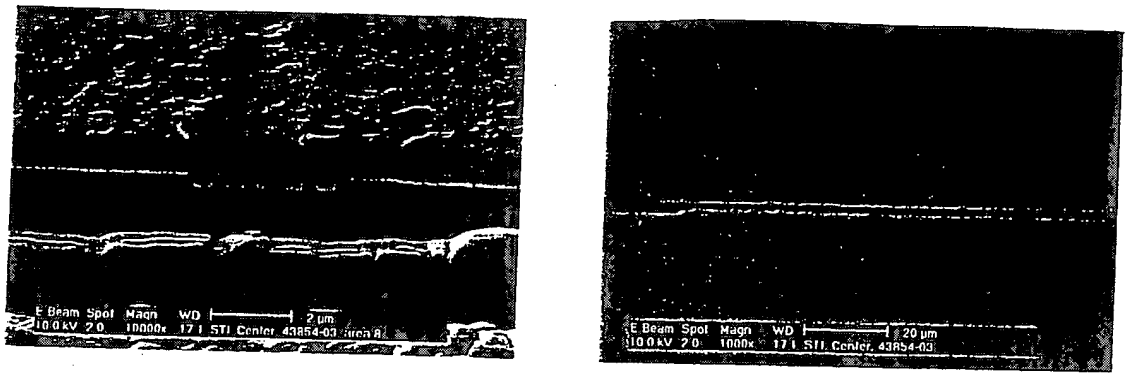

FIG. 17

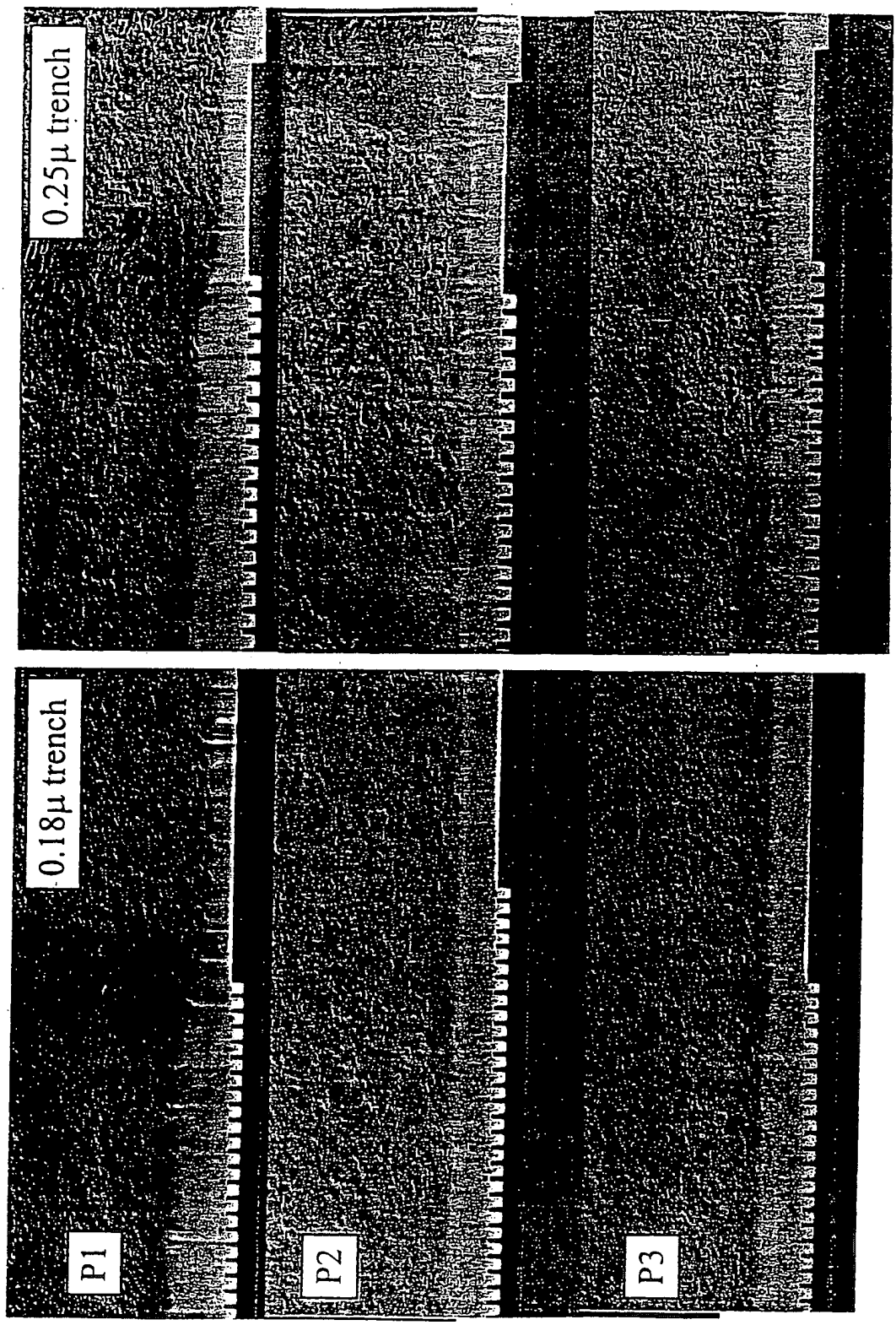

FIG. 18

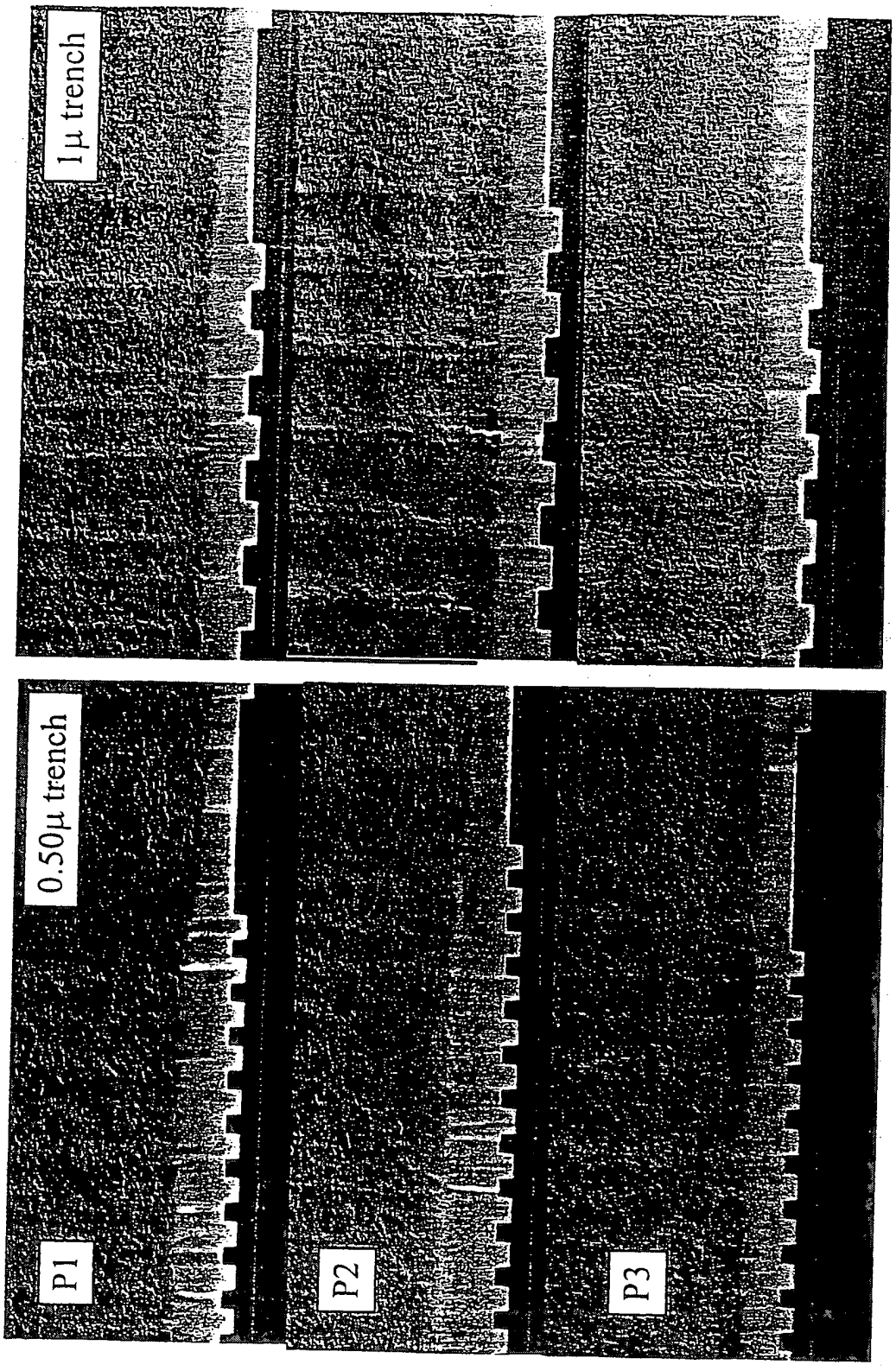

FIG. 19

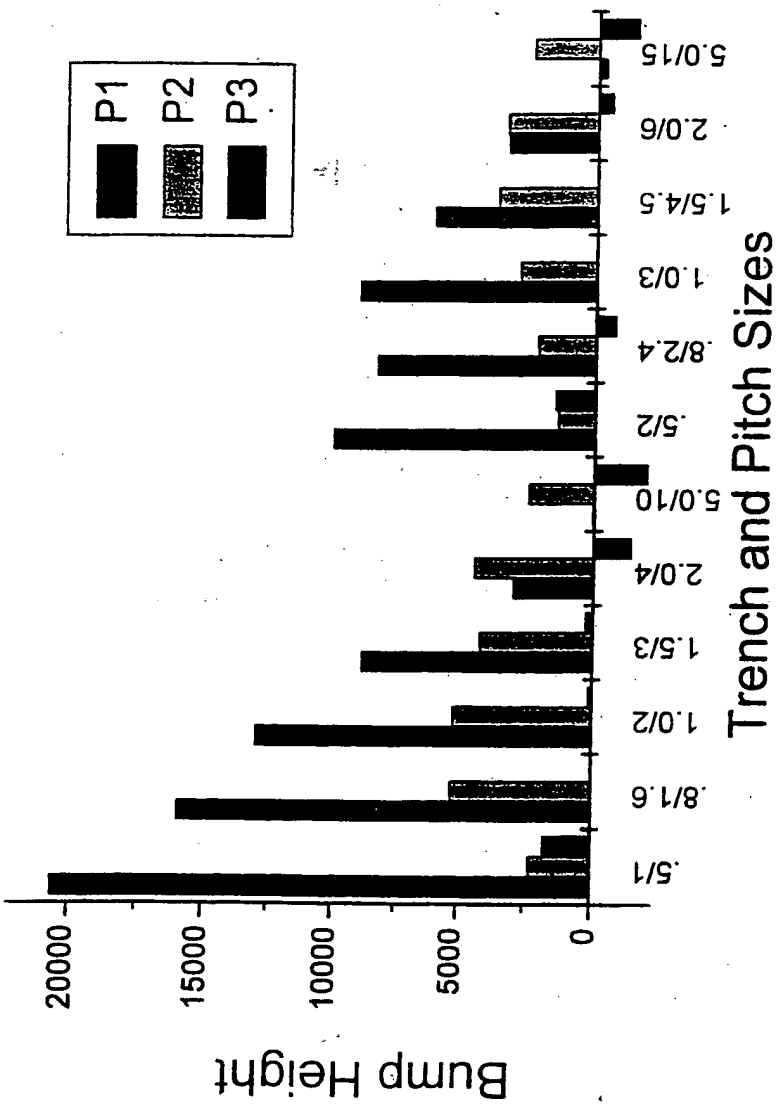
P1
P2
P3
Bump Height
20000
15000
10000
5000
0
.5/1
.8/1.6
1.0/2
1.5/3
2.0/4
5.0/10
.5/2
.8/2.4
1.0/3
1.5/4.5
2.0/6
5.0/15
Trench and Pitch Sizes

FIG. 20

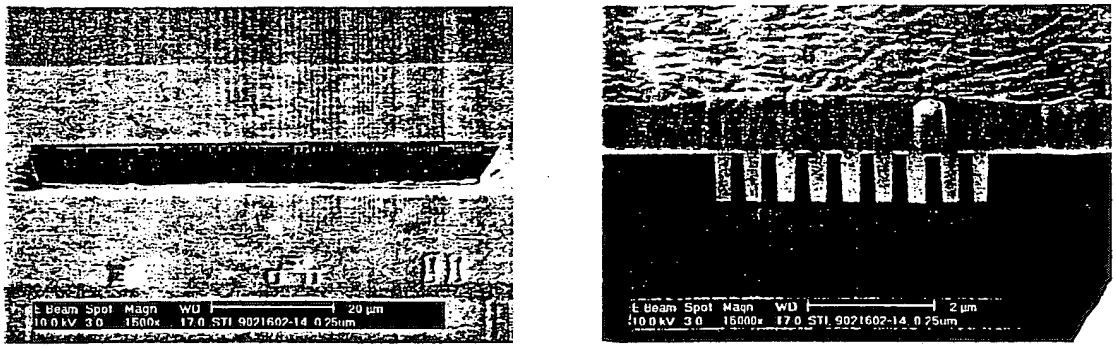

FIG. 21

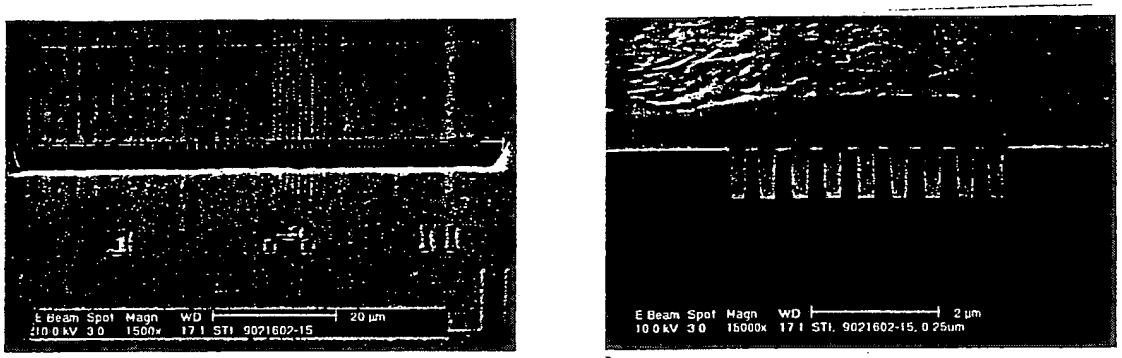

FIG. 22

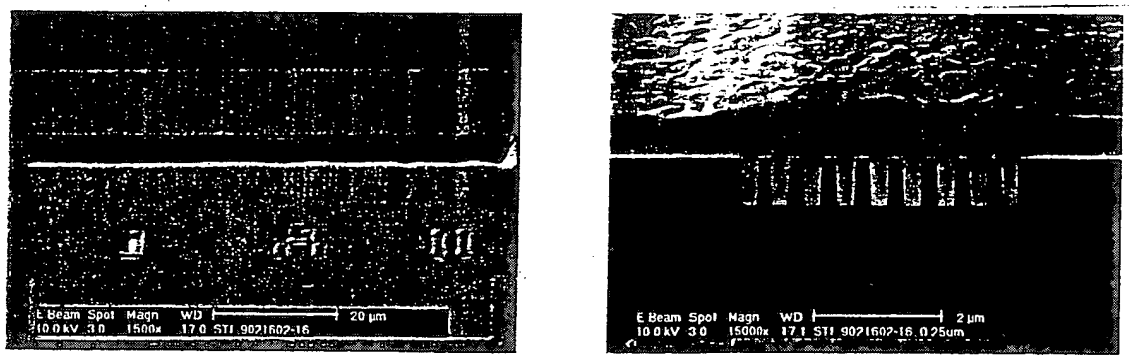

FIG. 23

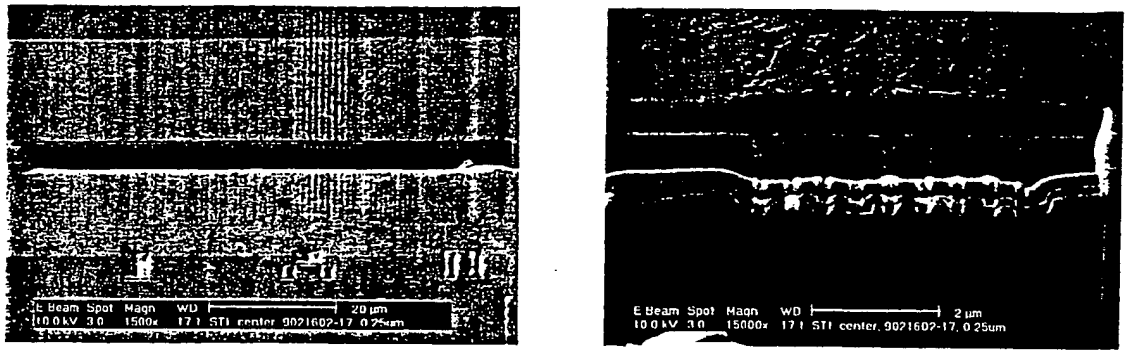
E Beam Spot Magn WD 20 µm
10.0 kV 3.0 1500x 17.1 STI center 9021602-17 0.25um
E Beam Spot Magn WD 2 µm
10.0 kV 3.0 15000x 17.1 STI center 9021602-17 0.25um

FIG. 24

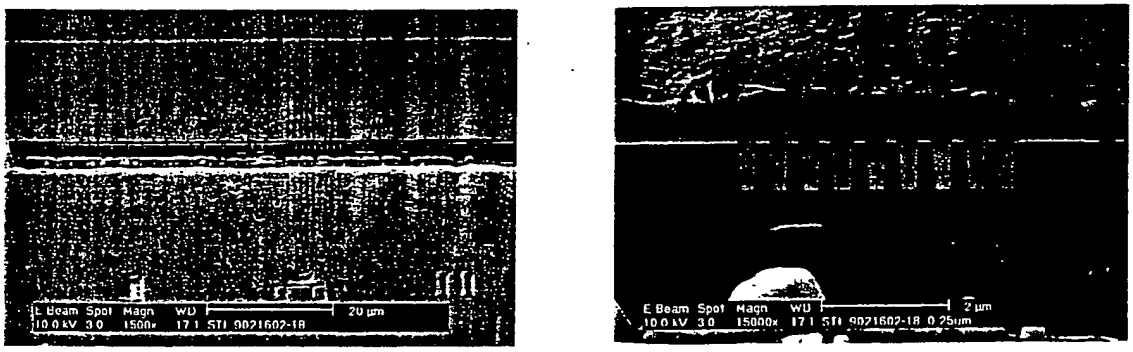
E Beam Spot Magn WD 20 µm
10.0 kV 3.0 1500x 17.1 STI 9021602-18
E Beam Spot Magn WD 2 µm
10.0 kV 3.0 15000x 17.1 STI 9021602-18 0.25um

FIG. 25